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Substrate Effects And Dielectric Integration In 2d Electronics

Bhim Prasad Chamlagain
Wayne State University,

SUBSTRATE EFFECTS AND DIELECTRIC INTEGRATION IN 2D ELECTRONICS

by

BHIM PRASAD CHAMLAGAIN

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DEDICATION

Dedicated to the memory of my mother

Tika Devi Chamlagain who gave me everything

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TMD: transition metal dichalcogenide

2D: two-dimensional

FET: field-effect transistor

hBN: hexagonal boron nitride

OTMS: octadecyltrimethoxysilane

SAM: self-assembled monolayer

SiO_2: silicon dioxide

Al_2O_3: aluminum oxide

Ta_2O_5: Tantalum oxide

TiO_2: titanium dioxide

MoS_2: molybdenum diselenide

$MoSe_2$: molybdenum disulphide

WSe_2: tungsten disulphide

BP: black phosphorus

Si: silicon

PPMS: physical property measurement system

SEM: scanning electron microscope

AFM: atomic force microscope

CVD: chemical vapor deposition

ALD: atomic layer deposition

NPGS: nano patterning generation system

PMMA: polymethyl methacrylate

HSQ: hydrogen silsesquioxane

IPA: isoproponal

DFT: density functional theory

STM: scanning tunneling microscope

STS: scanning tunneling spectroscope

MIBK: methyl isobutylketone

MEK: methyl ethyl ketone

SS: subthreshold swing

PDMS: Poly-dimethylsiloxane

RT: room temperature

MIT: metal insulator transition

SB: Schottky barrier

CMOS: complementary metal-oxide semiconductor

ROP: remote optical phonon

XPS: X-ray photoelectron spectroscopy

EDS: Energy dispersive spectroscopy

UHV: ultra-high vacuum

CHAPTER 1 GENERAL INTRODUCTION

1.1 TWO DIMENSIONAL MATERIALS

Two dimensional (2D) materials with atomic thicknesses have recently attracted tremendous interest from the scientific and engineering communities. The most studied 2D materials to date are graphene, hexagonal boron nitride (h-BN), black phosphorus (BP) and transitional metal dichalcogenides (TMDs) such as molybdenum disulphide (MoS_2), tungsten diselenide (WSe_2) and molybdenum diselenide ($MoSe_2$). These 2D materials have displayed varying electronic properties ranging from metal, to semiconductor, insulators and even superconductor. Among 2D semiconductors, different band gaps, charge neutrality levels, and spin properties have been observed, which offers the versatility for the development of 2D electronics, optoelectronics and spintronics.2Dmaterialsare promising candidates for a wide range of applications from nanoelectronics, optoelectronics, sensing, photonic[1]. Particularly, these atomically thin films are ideal channel materials for nanoscale flexible electronics applications, such as low power, high-frequency, and flexibledevices.[1-3] Graphene is the most widely explored 2D material because of its extremely high carrier mobility and unique physical properties. In addition, the synthesis of large area graphene films using chemical vapor deposition (CVD) is also feasible. In spite of the favorable mechanical, thermal, electronic and optical properties, graphene is a zero band-gap semiconductor. As a result, graphene transistors typically exhibit a very low on/off current ratio, which makes grapheme a poor channel material in logic electronics. Sustained efforts to open up a band gap in graphene have either caused severe mobility degradation or require prohibitively high bias voltages.[4]Solayered transition metal dichalcogenides (TMDs) and black phosphorous (BP) have emerged as a viable alternative to grapheme because they combine a semiconducting gap with mechanical flexibility, chemical

& thermal stability and absence of dangling bonds. Low energy devices, digital electronics & optoelectronics based on these materials have been demonstrated in recent studies.[5-19] Similar to graphene, atomically thin layers can be easily produced by mechanical exfoliation from their bulk crystals because of the weak van der Waals forces between adjacent layers.

1.1.1 TRANSITION METAL DICHALCONIDES (TMDs)

The transition metal dichalcogenides have chemical composition described by the formula MX_2 (M = Ti, Zr, Hf, V, Nb, Ta, Cr, Mo, W, Pt and X = S, Se, Te). The properties of transition metal dichalcogenidesvaries from metal (NbS_2, TiS_2, TaS_2, VSe_2), semimetal (like WTe_2, TeS_2), semiconductor (like MoS_2, $MoSe_2$, WSe_2) to insulator (like HfS_2).[20] The transition metal dichalcogenides (TMDs) have layered structure with two general configuration of either trigonal prism or octahedron having different lattice symmetries.[21] MX_2crystals are hexagonally packed with stacking layers of X–M–X. The bond between two-dimensional X–M–X layers is covalent type and stronger than the interaction between the atoms residing on different planes, which is van der Waals type and is relatively weak. The strong covalent bonds between transition metal and chalcogen atoms on the plane and weak van der Waals bond between layers allows making atomically thin layer by micromechanical cleavage method by splitting the layer by layer structure. The unique properties of TMDs including chemical & thermal stability, mechanical flexibility, ultra-smooth atomic thickness, absence of dangling bonds& interface traps, sizeable band-gap, reasonably high carrier mobility and fast growing synthesis techniques have been attracted researchers a lot of interest to implement the revolutionary applications in novel transparent & flexible electronics[1, 22], optoelectronics[1], stacked van der Waal superlattices & heterojunctions[23], spintronics (valleytronics)[24-27] and ultimate atomically thin field effect transistors.[2, 28] **Fig.1.1.1** shows the periodic table with highlighted columns for transitional

metals and chalcogens, by combining them about 40 different layered TMD compounds exists and their possible crystal structures. Only some dichalcogenides of partial highlights of transitional metals form layered structure. For example, NiS_2 is found to have apyrite structure which is not layered structure but $NiTe_2$is a layered dichalcogenide. Right side of **Fig.1.1.1** shows the two possible crystal structures of transitional metal dichalcogenides. The layer structure has hexagonally packed layer of metal atoms sandwiched between two hexagonally close packed chalcogen atoms with intra-layer bonds are covalent and interlayer bound force is van der Waals. The thickness of single layer TMD is about 6 to 7 Å. Each metal atom provides four electrons to two chalcogen atoms to form TMD layer structure such that the oxidation state of metal is +4 and the oxidation state of chalcogen is -2. The TMD layer structure has absence of dangling bond because the lone pair electrons of chalcogen atoms terminate on the surfaces of layers. Bulk TMDs exhibit a wide variety of polymorphs in which most common polymorphs are 1T, 2H and 3R where the letters stand for trigonal, hexagonal and rhombohedral, respectively. For instance, natural $MoS_2$is commonly found in the 2H phase where the stacking sequence is aBabAb in which the upper case letters represent metal atoms and lower case letters represent chalcogen.On the other hand, synthetic MoS_2often contains the 3R phase where the stacking sequence is aBacAcbCb. In both phases, the metal coordination is trigonal prismatic. Some of the TMDs such as $TiS_2$are 1T phase where the stacking sequence is aBcaBc and the coordination of the metal is octahedral. Recent experimental report demonstrated that the metallic 1T phase of MoS_2 can be locally induced on semiconducting 2H phase nanosheets.[29] Because of its layer structure, single layer/few layers TMDs can be easily exfoliated from bulk crystal by mechanical cleavage method.

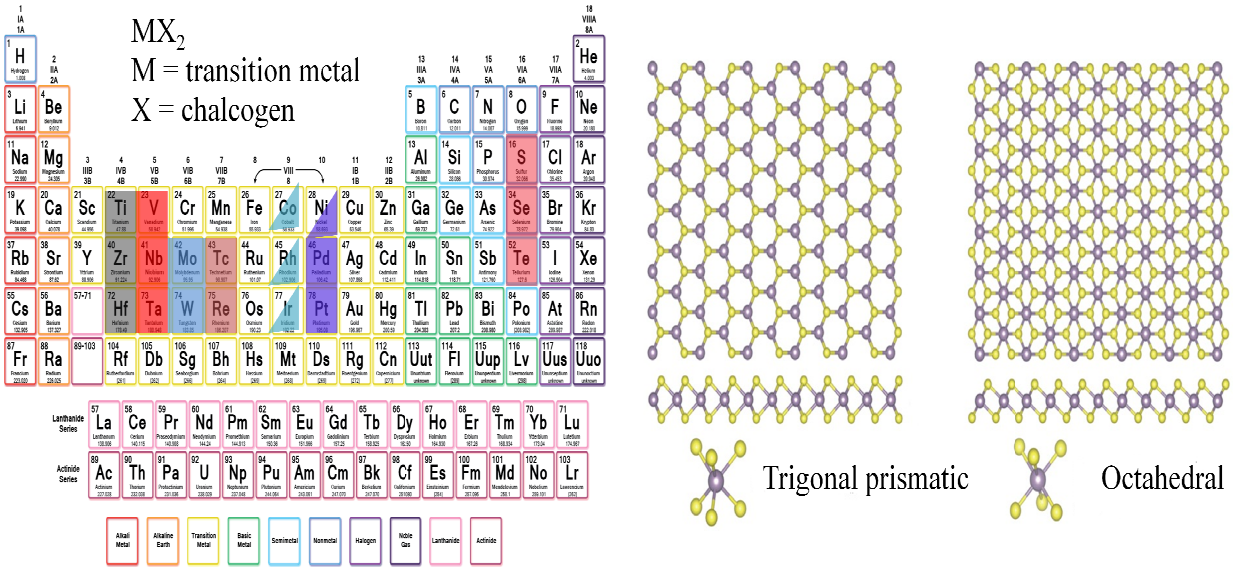

Fig.1.1.1 The left picture is periodic table which shows the transition metals and the three chalcogen elements that predominantly crystallize in those layered structure are highlighted in the periodic table. Middle and right pictures are the axis and section view of single-layer TMD with trigonal prismatic and octahedral structures in which purple color represents transistion metal atom and yellow color represents chalcogen atom.

Table 1.1.1 shows the some of the possible transitional metal dichalconides. The bulk form of these materials form indirect band gap and changed to direct band gap for monolayer due to quantum confinement.[1, 30] Due to the difference of band gap and direct gap nature of monolayer TMDs compared to its bulk form opens up platform to investigate different interesting properties of monolayer TMDs and their possible applications.

Material	E_g in bulk (eV)	E_g monolayer (eV)
MoS_2	1.2	1.8
$MoSe_2$	1.2	1.5
WS_2	1.4	1.9-2.1
WSe_2	1.2	1.7
$MoTe_2$	1	1.1
WTe_2	0.7	1.1

Table 1.1.1 Some of the semiconducting TMD materials and their band gap

1.1.1.1 MOLYBDENUM DISULFIDE

Molybdenum is a transition metal element from group **VI** and sulphide is chalcogen (oxygen group). The mineral of MoS_2 called *molybdenite* is exists in nature. MoS_2 has three different structural phases. The first one is 2H-phased MoS_2 which has hexagonal symmetry and semiconducting properties. It is found in nature and having layer structure which can be easily mechanically exfoliated into few layers to single layer. The second one is 1T-phased MoS_2 having tetragonal symmetry which has metallic properties. The third one is 3R-phased MoS_2 with rhombohedral symmetry which has semiconducting properties like 2H-phased MoS_2. Semiconducting MoS_2 has indirect band gap with 1.2 eV in bulk form and change into direct band gap 1.8 eV for monolayer due to quantum confinement.[1] In the past, MoS_2 is used as a lubricant because of its lubricating property.

1.1.1.2 MOLYBDENIUM DISELENIDE

Molybdenum is a transition metal element from group **VI** and Selenium is chalcogen (oxygen group). Molybdenum diselenide ($MoSe_2$) is a transition metal dichalcogenides having similar structure as other TMDs. $MoSe_2$ forms layered structured of the form Se - Mo - Se with selenium atoms in two hexagonal planes separated by a plane of Molybdenum atoms. The strong covalent bond exists between Molybdenum & Selenium with weak interlayer coupling by weak van der Waal force. In $MoSe_2$, the metal atom has trigonal prismatic coordination within the sandwich layer and a number of stacking polytypes are possible depending upon the way in which the sandwich layers are stacked one upon the other. Bulk $MoSe_2$ shows semiconducting behavior with indirect band gap 1.1 eV. The indirect band gap of bulk $MoSe_2$ changed into direct band gap 1.5 eV for monolayer $MoSe_2$.[1]

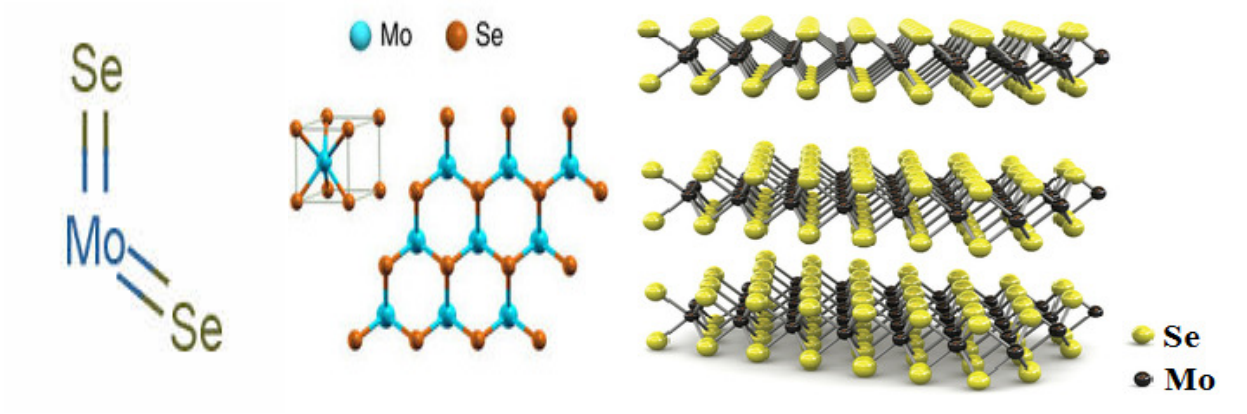

Fig.1.1.2 $MoSe_2$ general bond formation structure, schematic representation of unit cell and honey comb structure of $MoSe_2$ structure and three-dimensional schematic representation of $MoSe_2$ structure.

1.1.2 BLACK PHOSPHORUS

Black phosphorus (BP) is thermodynamically stable allotrope of phosphorus at room temperature and pressure. It is elemental semiconductor with anisotropic crystal structure. It is looks like black in color and orthorhombic, buckled structure with each phosphorous atom have one bond along armchair direction and two bonds along zigzag direction as shown in **Fig.1.1.3**. It forms layer structure as like graphite and can be exfoliated to monolayer called phosphorene by mechanical exfoliation method. The band gap of bulk BP is 0.3 eV and increase up to 2 eV for monolayer while its few-layer structures have thickness-dependent direct band gaps between 2 eV to 0.3 eV.[31-34] With advancement of mechanical exfoliation method BP opens up new opportunities for electronic and optoelectronic applications. Especially reported high mobility reported favorable for electronic application and the variable direct band gap for monolayer to bulk is suited optoelectronic application. Unlike other 2D materials, the electrical, optical, mechanical and thermal properties of BP show anisotropic nature due to its anisotropic crystal structure.[32, 35, 36]It has been found that the BP reacts with air in presence of water vapor which degrades its electrical properties gradually. The degradation enhances in presence of light.[37, 38]

The chemical degradation of BP at ambient condition challenges the researchers to prevent to contact with air, water and light for preserving it pristine properties.

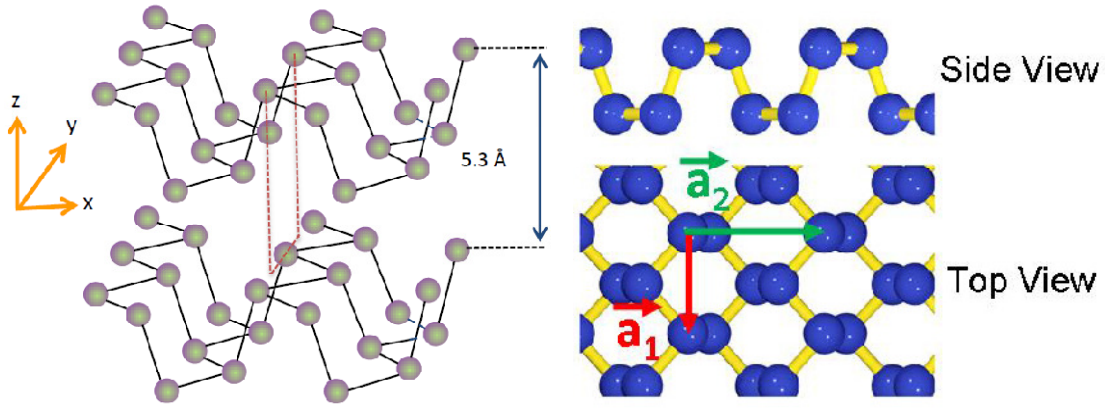

Fig.1.1.3 Layered crystal structure of black phosphorus with two adjacent puckered sheets. Side and top view of few layer black phosphorus is on the right side of the figure.

1.2 SYNTHESIS OF 2D MATERIALS

Reliable and reproducible synthesis of atomically thin 2D materials with uniform properties is essential to study their intrinsic and extrinsic properties. High purity and cleanliness of flakes/films are essential to study fundamental properties of 2D materials. Complex fabrication process and materials/chemicals used in fabrication process might introduce impurities on the 2D flakes which might alter the intrinsic properties. Some of the common established methods to get 2D materials are as follow:

Top-down method: This is the method of preparation of atomically thin 2D materials from bulk crystal. Atomically thin layer as well as few layers of 2D material from its bulk crystal can be prepared by micromechanical cleave method as first time done to prepare graphene.[16] The bulk crystal is kept on scotch tape and exfoliates by using another scotch tape. By cleaving multiple times using adhesive scotch tape, thin enough flakes can get on scotch tape. By introducing substrate on the scotch tape having thin layers of 2D materials, sufficiently thin 2D flakes can be transferred to substrate. 2D materials having different thickness on a substrate

show different optical contrast with visible light. This property is used to find the atomically thin flakes with interference of visible light on it by using optical microscope.[39, 40] The light interference is caused by reflection/refraction of thickness of 2D layer and substrate thickness. This method produces atomically thin 2D flakes of high purity and cleanliness as bulk crystal but it is not control over dimensions. So, it is hard to control thickness and size of 2D flakes systemically. More strictly speaking, it is hard to get large thin flakes with appropriate size and dimensions. Another top-down method to get atomically thin 2D material from its multilayer is laser-induced thinning.[41] The multilayer of crystal is exposed by laser with required exposition dose which is controlled by adjusting the incident laser power, the step size and the exposure time. This is a reliable method to get atomically thin 2D layers with user-defined shape and size but the roughness of the laser scanning surface is main problem and the requirement of adjustment of parameters of laser scanning is challenging. The interaction of chemical with bulk crystal is used to exfoliate the bulk crystal into atomically thin 2D flakes called chemical exfoliation method. This method produces required monolayer but the resulting 2D material may have different structure and electronic properties from the bulk material.[13] The chemical used to exfoliate the sample might change the intrinsic properties by introducing charges and other impurities.

Bottom-up method: The process of getting atomically thin layer of 2D materials starting from zero thickness is bottom-up method. Chemical vapor deposition (CVD) is one of the well-known preparation of 2D material layer.[42,43] This method gives large flake size. But the control over flake thickness and quality of the flake is challenging. Repetition of the process to get similar flakes with right size and thickness is still challenging. The crystal growth depends upon different parameters including the external environment which creates challenges to keep same

condition during growth process. Particular recipe for CVD grown of certain 2D material is substrate dependence. Different recipe should be used to grow same material on different substrates.

1.3 TRANSPORT PROPERTIES AND DEVICE PERFORMNCE OF 2D SEMICONDUCTORS

Transport properties of 2D semiconductor shows wide variation depending up on their materials, type of charge carriers and dielectric used. The studies of graphene have revealed its exceptional electronic properties based on the unique band structure including the observation of ambipolar behavior. The charge carriers in graphene can be described as relativistic particles called Dirac fermions by Dirac equation for this 2D crystal, providing a way to explore quantum electrodynamics (QED).Graphene has reported high mobility, exceed 15000cm^2 V^{-1} s^{-1} at room temperature with ballistic transport, and shows quantum Hall effect.[8, 44] On the other hand, the electron mobility values of monolayer and multilayer MoS_2 devices on SiO_2 reported by multiple groups were substantially below the Hall mobility of bulk MoS_2 (100 - 200 cm^2 V^{-1} s^{-1}).[2, 45, 46] Bao at. al. reported ambipolar multilayer MoS_2 with two terminal field-effect mobility attained to 470$cm^2V^{-1}s^{-1}$ at room temperature on PMMA but the improvement of mobility is still unclear.[47] S. L. Li et.al. presented thickness dependent interfacial charge scattering of MoS_2 FET and showed the improvement of field effect mobility with increase of thickness by suppressing the Coulomb scattering originated from SiO_2 surface and MoS_2 /SiO_2 interfaces.[48] Different efforts to modify the SiO_2 surface, using high-k dielectric such as HfO_2, $Al_2O_3$and h-BN encapsulation have been done for graphene and TMDs field effect transistor but the mobility values never reached to theoretical phonon limited mobility[45, 49-53], which indicates the carrier mobility of 2D channel materials is limited by extrinsic scattering from charged impurities at the

channel/substrate interface and charge traps in dielectric, substrate surface roughness, and remote surface optical phonons originating from substrate.

A good transistor layer material should have enough high charge carrier mobility for high on state current and fast operation of transistor. The layered materials should have reasonable band gap to maintain enough on/off current for the operation of transistor by electrostatically switching on and off state. On the other hand, sharp switching characteristic is equally important to allow high degree of electrostatic control over devices. To achieve all of these ideal properties, selection of channel materials and dielectric materials is exceptionally important. In addition, devices structures, designs and modification are also important to optimize and modify the 2D thin layer transistor devices properties.

1.4 FACTORS RELATED TO TRANSPORT PROPERTIES OF 2D SEMICONDUCTORS

The channel of 2D materials is thin which needs substrate to support and for the investigation of its properties we have to connect with metal electrodes. The contact metal form barrier with semiconductor channel of 2D materials and the dielectric on substrate plays important role to determine the channel properties of the thin 2D materials. Basically there are following main challenges which have to address to investigate the channel properties and optimize the 2D based semiconductor electronics.

1. contact effect
2. interface effect
3. dielectric integration

My main focus of the work is details interface effect study of 2Ds based semiconductors field effect transistor (FET) and 2D heterostructure integration to optimize the performance of FET with dielectric integration. To reveal these effects, we have to start the basic concept of

common scattering mechanisms of 2D materials and external factors which affect to investigate the intrinsic properties of 2D thin flakes.

1.4.1 SEMICONDUCTOR AND ELECTRODE (METAL) CONTACT

Metals leads need to be connected to study the channel properties of 2D semiconductor flakes. But there is formation of schottky barrier at metal semiconductor junction. The schottky barrier can be successfully eliminated by adopting the transfer line method or four terminal measurements but practical FETs are two terminal electrodes as drain and source which greatly affected by schottky barrier and limit the performance of the device. Scottky barrier due to band off set of metal semiconductor, Fermi level pining due to the interface states of semiconductors and current crowding effect due to non-uniform injection of charge carriers along the entire metal/semiconductor length are the main problems to device performance of 2D semiconductors FET.

1.4.2 CARRIERS SCATTERING MECHANISMS

In 2 dimensional TMDs layers, transport and scattering phenomena of the charge carriers are confined to the plane of the material and on the surface of the substrate. In these ultrathin 2D channels, the interface effects are particularly important. The mobility of charge carriers is mainly determined by following mechanisms: [51, 54-57]

(a) Lattice or phonon (acoustic & optical phonon) scattering.

Energized phonons within the 2D materials couple with charge carriers and affect the motion of charge carriers. Optical phonon scattering is dominated factor at high temperature. So the charge carrier mobility is largely affected by phonon scattering with increase of temperature.[58] The phonon vibrations within the TMD channel includes out of plane homo-polar mode and in plane phonon vibration. Depending upon its vibration energy, it can be excited by

thermal energy. Some of the phonon has enough low excitation energy which is sufficient to excite by thermal energy at room temperature or even lower. The quenching of thermally excited phonon is efficient method to reduce its effect on transport property of 2D TMDs. The out of plane homo-polar phonon mode vibration can be quenched by sandwiching the vibration between top gate dielectric and back gate substrate.

(b) Atomic and structural defects scattering

It is really challenging to grow a crystal without defects. Although naturally occurred TMDs crystals are relatively low lattice defects, the commercially grown TMDs monolayer TMDs crystals have abundant crystal defects.[59] The lattice defects form scattering centers for charge carriers and scatter the accelerated charge on the channel. Lattice defects also promote the foreign materials to add and form scattering centers for accelerated charge particles.

(c) Coulomb scattering.

It is common to introduce charge impurities during the fabrication process of 2D materials since it is in contact with other materials like PDMS, PC, PMMA and many other chemicals in the process of making devices. Moreover, the substrate itself introduces trap charges between 2D materials channel and substrate. The substrate surface and 2D materials may trap the water, air bubble and other foreign materials as a source of charge impurities. Due to the Coulomb force between the charge carriers and random charge impurities which are located within the layered TMDs & on its surface causes the Coulomb scattering. Coulomb scattering is also caused due to charge impurities and charge traps at the interface between TMDs & substrate. The polar molecules on the surface of the substrate set up electric field around it which creates additional Coulomb scattering of charge carriers along TMDs channel. It has dominant effect at relatively low temperatures at which the phonon scattering is insignificant.[60, 61] Gate

dielectric materials play an important role to modify the effect of coulomb scattering due to charge impurities. Non-polar dielectric having inert and smooth surface is an ideal material to decrease the Coulomb scattering. Argument of dielectric screening of Coulomb scattering on charge impurities is recently introduced for MoS_2 transistor by using gate dielectric material having high dielectric constant.[2] The coulomb scattering from the interface of substrate and TMDs channel and coulomb scattering introduced from substrate is crucial for thin layer of TMDs channel. Recently more severe scattering from charge impurities on single layer MoS2 channel is reported from the study thickness dependence coulomb scattering.[61]

(d) Surface roughness scattering.

Different substrate has different roughness depending upon its atomic arrangement on the surface, surface growth quality etc. It is important to consider the effects of smoothness of the substrate to study the channel properties of ultrathin 2D materials in back gate configuration. The charge carriers, which are concentrated close to the substrate due to the applied back gate, are scatter from the surface of the substrate. Rougher surface enhances the charge carriers scattering from the surface. The roughness of the substrate and the sample surface roughness as ripples can play important role for mobility deterioration of charge carriers in 2D materials as well as its transport properties.[62]

(e) Surface interfacial phonon scattering

Surface phonons are particular lattice vibration modes associated with vibration of molecules/atoms of substrate surface. Surface phonons on the surface of the substrate can couple with charge carriers through TMD channel and affect the electrical and optical properties of devices. Since the thickness of 2D TMDs is atomically thin, the effect of surface polar phonon scattering is also significant. The polar molecules on the surface of the polar substrate (as SiO_2)

create electric field as shown in **Fig. 1.3.1**. The charge carriers inside this field can be scattered by the polar phonons.[54] The effects of surface phonon can be investigated by using different dielectric materials having various surface phonon energies like SiO_2, PMMA, Al_2O_3, hBN, HfO_2, TiO_2, Ta_2O_5.

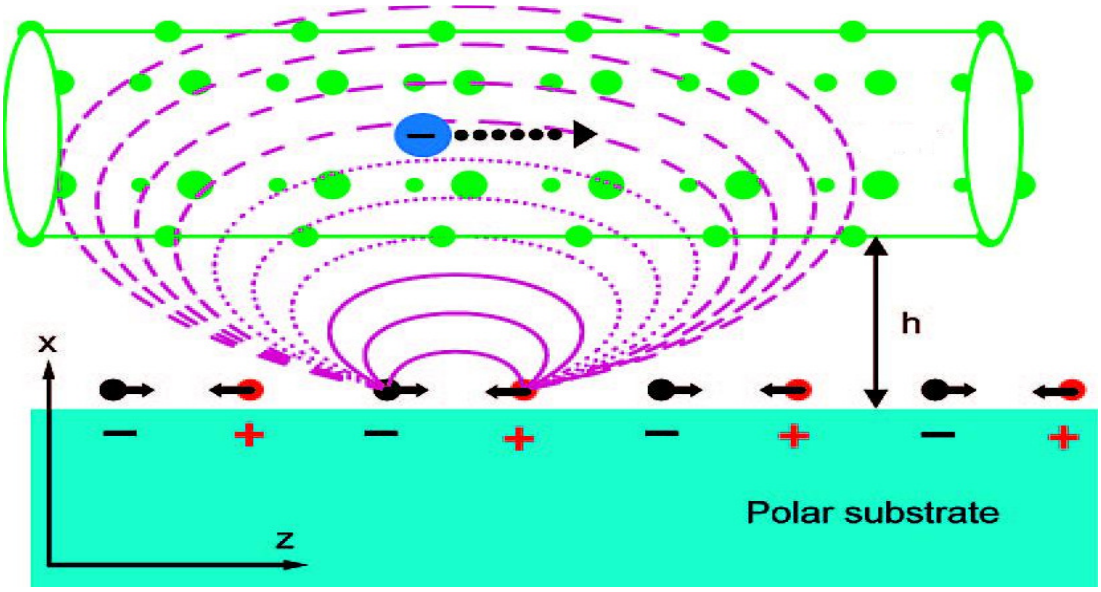

Fig. 1.4.1 Schematic diagram of electric field developed in the vicinity of polar substrate surface

Substrate dielectric has great influence to determine the transport properties of TMDs channel. So it is better to distinguish the charge carriers scattering factors in terms surface induce and channel induce. Scattering mechanisms are classified into two categories in terms of the scattering factors from channel and substrate.

Scattering mechanisms from the channel materials

- Optical phonons scattering due to intrinsic phonon
- Acoustic phonons scattering due to intrinsic phonon
- Scattering due to structural defects in the channel material
- Coulomb scattering due to impurities in the channel

Scattering mechanisms from the channel materials

- Coulomb scattering due to charged impurities at the interfaces/substrate
- Phonon scattering due to remote surface optical phonons
- Roughness scattering due to interface roughness

Substrate plays crucial role to deviate from intrinsic properties of the channel material. So it is worth to study the details of different scattering mechanism caused by substrate.

Besides these factors, the schottky barrier height plays important role to deteriorate the extrinsic mobility of the charge carriers. The extent of effect to the mobility of charge carrier by these mechanisms is also influenced by other factors like temperature, dielectric environment, effective mass of charge carrier, electronic band structure, thickness of the layer, charge carrier density.[1]

One of the most promising applications of thin 2D materials is field effect transistor (FET). The most desirable features of FETs are high carrier mobility, high ON-OFF current ratio, presence of both electron and hole conduction, high optical transparency, thermal & chemical stability, and mechanical flexibility.[63] The 2D layered materials might be best candidates for the FETs in order to meet these requirements.

Low resistance contacts and substrate effects are critical to investigating the channel properties of ultrathin 2D materials. Also we are using the four-wire method which demands low contact resistance for the validity of measurements. Choice of different substrate helps to reveal the substrate effects on channel of ultrathin 2D materials.

In my study, I mainly focus on the study of substrate effects, dielectric environment effects, contact effects and thickness dependence on electrical transport properties of ultrathin TMDs FET and dielectric integration of 2D materials. I focus on 2D materials MoS_2, $MoSe_2$, Black Phosphorus as channel materials with different types of dielectric combinations of SiO_2,

OTMS SAM modified SiO_2, Al_2O_3, hBN, parylene-C and other dielectric synthesis from 2D layer structure to study the substrate effects, dielectric environment effects and thickness dependence on electrical transport properties of ultrathin TMDs FET. For the contact effect study, I chose 2D materials MoS_2, $MoSe_2$, WSe_2 as channel materials and their p (n) doping as 2D contact materials.

1.5 DIELECTRIC INTEGRATION

Dielectric is extremely crucial for 2D semiconductor. Both scientific and technological issues like the choice of dielectric material, their deposition, their structural and metallurgical behavior, atomic diffusion, interface structure and reactions, their electronic structure, bonding, band offsets, electronic defects, charge trapping and conduction mechanisms, mobility degradation and flat band voltage shifts are the essentials factors to consider for selecting the appropriate dielectric. Vacancy state in dielectric is the dominant electron traps which directly and indirectly responsible for external scattering of charge carriers in 2D semiconductor channel. A systematic consideration of the required properties of gate dielectrics indicates that the key guidelines for selecting an alternative gate dielectric are permittivity, interface quality, interface properties, band gap, and band alignment to 2D semiconductor, thermodynamic stability, film morphology, compatibility with the current or expected materials to be used in processing for complementary metal oxide semiconductor (CMOS) devices, process compatibility, reliability, and maintenance of a high charge carriers mobility in the channel and minimization of electrical defects in the film/interface. Few layer 2D materials have extremely sensitive large area. The charge impurities introduce on the surface at the dielectric interfaces causes coulomb scattering which significantly degrades the transport properties especially carriers mobility. The ambient exposure of the 2D materials surface shows completely different transport mechanism and also

causes surface chemical degradation. Defects in crystal like grain boundaries and point defects severely change the properties of the 2D materials devices. Numerous challenges exist for 2D materials that prevent large-scale integration into its applications.

On the other hand, a practical transistor channel material should have high charge carrier mobility, reasonable band-gap, and low subthreshold swing (SS) to compete with complementary metal oxide semiconductor. High charge carrier mobility is needed for high speed operation of transistor with high on current. In the meantime, it should have reasonable band-gap to get a very low current at off state. In addition, lower subthreshold swing is extremely desirable for much needed electrostatic control of transistor. Moreover, the size of the transistor should be very small for the fast growing industrial market.

If the size of the transistor is decreased, then the encroachment of electric field lines from drain/source causes the undesirable distribution of electric fields on channel by competing the available depletion charge. This attributes the decrease on/off ratio (increase off current) and subthreshold swing degradation (reduce the electrical control) called short channel effect. In this case, the electric field in the channel can be modeled using the Poisson distribution.[64]

$$\frac{d^2\phi(x,y,z)}{dx^2} + \frac{d^2\phi(x,y,z)}{dy^2} + \frac{d^2\phi(x,y,z)}{dz^2} = qN/\epsilon_{ch}$$

The solution of the Poisson equation gives characteristics length called natural length λ,

$$\lambda = \sqrt{\frac{\kappa_{ch}}{N\kappa_{ox}} t_{ch} t_{ox}}$$

Where κ_{ch} and κ_{ox} are dielectric constants of the channel and the dielectric oxide, t_{ch} and t_{ox} are the thicknesses of the semiconducting channel and the oxide, N is the effective gate number.

Natural length represents the penetration distance of the electric field lines from the drain/source in the channel of the device. It also represents the amount of control the drain/source region has on the depletion region, as both the gate and the drain compete for that control. So it gives a measure of the short-channel effect of the device structure. A device can be considered free of short-channel effects if the gate is at least six (5-10) times longer than λ.

As transistors have decreased in size, the thickness of gate dielectric has steadily decreased to increase the gate capacitance and thereby drive current, raising device performance by high degree of electrical control. But the decrease of gate dielectric thickness sets lower natural length which significantly increases the subthreshold swing as well as significantly degrades the electrical control over device. The implementation of high-κ gate dielectrics is one of strategy to overcome the problems. Using high-κ gate dielectrics gives higher natural length and helps to reduce the short channel effect. In addition gate dielectric with a high-κ material allow increased gate capacitance without the associated leakage effects and improve the field-effect charge carriers mobility of the channel by reducing Coulomb scattering.[11]

Besides these factors, we have to consider the surface optical phonon energy of the dielectric materials. The surface phonons can interact with charge carriers in the channel and cause severe remote surface phonon scattering. This external scattering significantly degrades the transport properties of the 2D semiconductor channel and reduces the charge carrier mobility. Selection of dielectric materials having high phonon excitation energy is the safest solution to reduce the surface phonon scattering.

1.6 SCOPE OF THE DISSERTATION

This dissertation focuses on fundamental properties of layered semiconductors, particularly, effects of dielectric properties, extrinsic impurities, and ambient absorbates on the

transport properties of ultrathin layered semiconductors. Chapter 2 introduces the working principles of the major characterization tools and techniques used throughout this research. To reveal the detailed extrinsic and intrinsic scattering mechanisms in MoS_2, we have fabricated MoS_2FETs on a wide range of substrates with different dielectric and surface properties and carried out variable temperature measurements in four-wire and Hall bar configuration as presented in chapter 3. In chapter 4, we present the structural characterization $MoSe_2$ crystal, FET device fabrication and detailed transport properties of $MoSe_2$. Chapter 5 introduces a novel 2D/2D vertical ven der Waals assembly method to achieve low-resistance ohmic contacts for TMD electronic devices. Chapter 6 reports the fundamental properties of black phosphorus (BP), which has drastically different band gap size and charge neutrality level than TMDs. Finally, chapter 7 includes the fabrication process for integration of high- k dielectric to TMDs based FETs and devices electrical characterizations.

CHAPTER 2 MAJOR EXPERIMENTAL TECHNIQUES

2.1 OPTICAL MICROSCOPE

An optical microscope uses visible light to magnify objects for observation. It uses a small and spherical objective lens which has a shorter focal length and another longer focal length lens called eyepiece. Object is placed near to objective lens and observes through eyepiece. The microscope brings an object's image into focus at a close distance within the tube by objective lens and eyepiece magnifies the image. Aside from a light source, a microscope also has a condenser which focuses light from the source to a small, bright spot of the specimen. It has fixed eyepieces and interchangeable objective lenses with different magnification. It can magnify incredibly small areas or object when the objective lenses are changed from flat with low magnification lenses to rounder with high magnification ones. The image quality seen by using an optical microscope is assessed based on brightness, resolution and contrast.

Optical microscope shows different contrast for different thickness 2D materials. The TMDs flake and other 2D flakes transfer on the substrate is observed under optical microscope to identify rough thickness of the better flakes. The optical microscope is used to estimate the thickness and identify the cleanness and uniformity of the sample.

Fig.2.1.1 Optical microscope

2.2 ATOMIC FORCE MICROSCOPE (AFM)

AFM is a kind of scanning probe microscope. A sharp probe called tip is moved close to the surface of sample under study in non-contact mode. The tip is connected to a cantilever. The tip scans across the sample surface and comes into force of interactions. As the cantilever is displaced by its interactions with the surface, the reflection of the laser beam will be displaced on the surface of the photodiode and the image is constructed. The surface topography is fully determined by the interacting forces during scan. AFM can measure a roughness of a sample surface, help to determine shape & the dimensions of sample, identify atoms at a surface, evaluate an interaction between a specific atom and its neighboring atoms, distinguish change in physical properties arisen from a change in an atomic arrangement through the atomic manipulation, help to distinguish cancer cells and normal cells based on a hardness of cells, evaluate an interaction between a specific cell and its neighboring cells in a competitive culture system.

The identified better sample flakes under optical microscope is characterized by non-contact mode XE-70 atomic force microscope (AFM). The surface topography of AFM image is analyses to determine the dimensions (length, width, thickness etc.), surface cleanness and surface roughness of the identified sample. XEI image processing software is used to process the AFM image. The surface smoothness is compare by root mean square value of PSD.

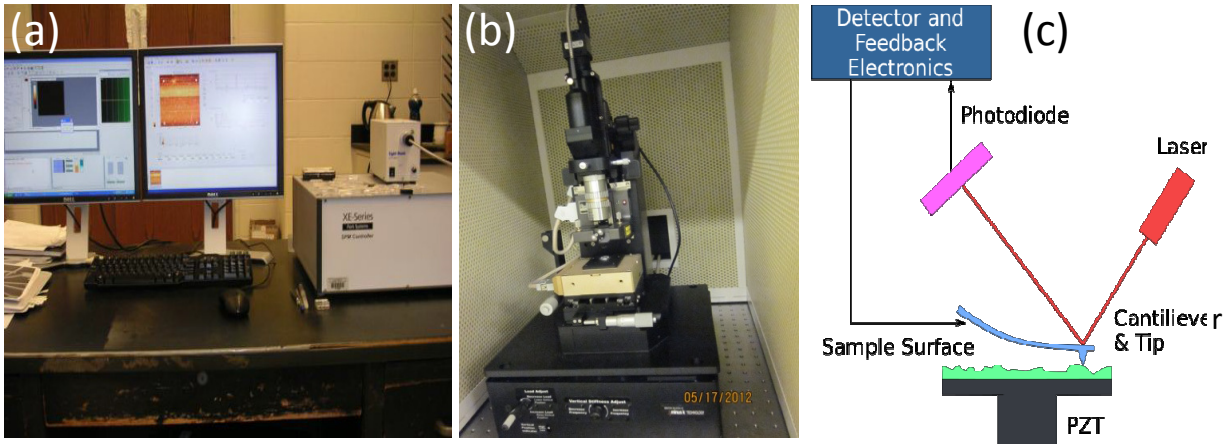

Fig.2.2.1 Atomic force microscope (Park Systems XE-70) (a) software system (b) the optical microscope and X-Y scanner as the main body(c) block diagram of AFM

2.3 SCANNING ELECTRON MICROSCOPE (SEM)

Although photo lithography is widely used in semiconductor industry, there are several other lithography methods developed in the past few decades such as X-ray lithography, electron beam lithography and ion beam lithography. E-beam lithography seems to provide appropriate way using electron as a source for making smaller feature size regarding feasibility and resolution since the diffraction limit has been an issue for photo lithography in current semiconductor technology in small feature size. Although slow speed and little costly are the drawbacks for e-beam lithography system, it has already been commonly used in semiconductor industry for patterning a smaller feature size.

In a SEM, a highly focused beam of electrons emitting from an electron gun is travel through a vacuum and are guided by electromagnetic lenses. The electrons beam hit the substrate surface coated by polymer and interact with it to break its bond. The polymer area which is interacted with electrons beam is easily soluble in organic solvent. We used Hitachi S-2400 SEM system with 25 kV maximum accelerating voltage to write the lithography patterns.

The selected better flake image is transferred to nano patterning generation system (NPGS) sketch and draws the desire electrodes as needed for different measurements configuration. Two layers of Polymethyl methacrylate (PMMA) polymer is coated on the substrate having sample and hit the collimated electrons beam to the specific area with specific design electrodes. In this work, we used Polymethyl methacrylate (PMMA) having two different molecular weight (PMMA 495-A4, PMMA 950-A2) as a positive resist and hydrogen silsesquioxane (HSQ) as negative resists for e-beam lithography. Then the substrate is dipped in MIBK/MEK solution (if PMMA as a resist) or CD-26 (if HSQ as a resist) to dissolve and open the specific design electrodes area PMMA polymer. The e-beam patterned substrate is coated by metal and defines metal electrodes to connect the measurement system.

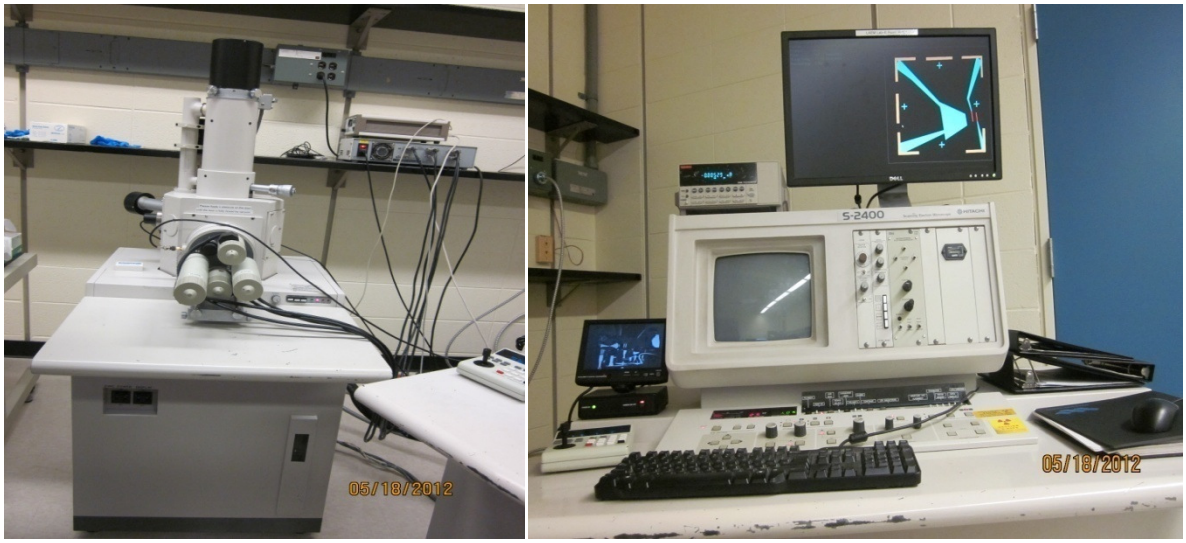

Fig.2.3.1 Scanning electron microscope (SEM) (Hitachi S-2400) set up for e-beam lithography.

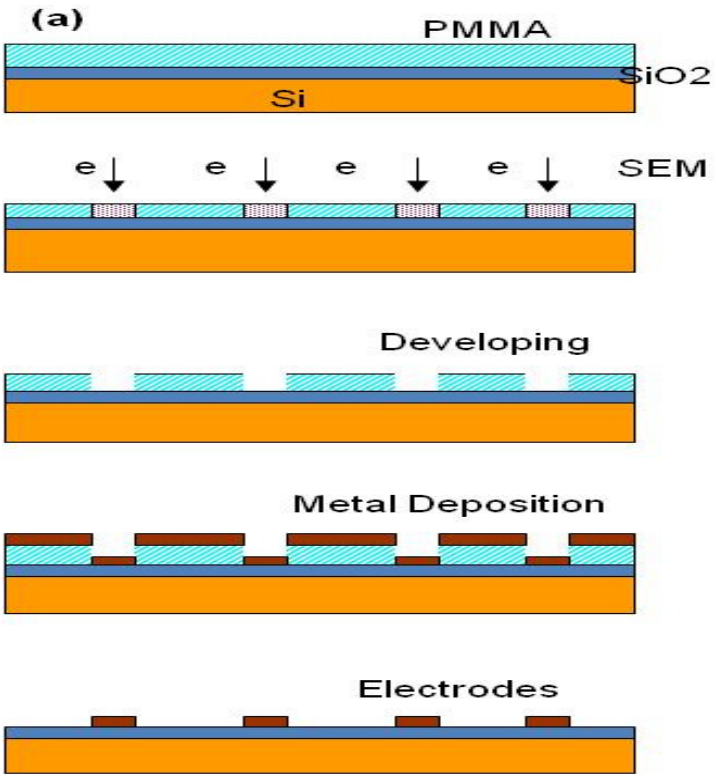

Fig.2.3.2 The schematic diagrams show the integrated processes with electron beam lithography and metal deposition, BJD 1800 e-beam metal evaporator

In terms of response to the electrons, polymers used in e-beam lithography are divided into two types, positive and negative. Positive resists are easily removed in the solvent on the e-beam exposed areas due to broken cross link polymer by e-beam like polymethyl methacrylate (PMMA) which is the most commonly used polymer for e-beam lithography. Negative resists do not dissolve in the solvent on the e-beam exposed area. Negative resist like hydrogen silsesquioxane (HSQ) is sometimes used for the protective mask of written electrodes.

2.4 BJD 1800 e-BEAM METAL EVAPORATOR

BJD-1800 metal evaporator is used to evaporate the metals to tailor the electrodes. The electrodes defined device is adjusted horizontally on BJD chamber and pumps it down to pressure about ~10^{-6}torr and deposit metal electrodes with sufficient slow deposition rate. The

metal deposition is done by evaporating the metal normal to the substrate without rotation for easy lift off. E-beam with proper frequency and current to hit the targets metals (contained in crucible) and get the metal evaporated to deposited on the target areas.

Fig.2.4.1 BJD 1800 e-beam metal evaporator

2.5 ULVAC MILA-5000 ANNEALING TOOL

The residue introduces during the fabrication process is crucial to alter the transport properties of 2D channel materials. We use different organic polymer like PMMA, PDMS, PC during fabrication process as well as blue tape for mechanical exfoliation of the sample. The substrate and sample may absorb moister and air during fabrication process timeline which depends upon humidity of the lab along with time to fabricate devices. To remove the organic residues, moister absorbed and other residues during the sample/device fabrication process, annealing is done in high vacuum. Bare Si/SiO_2 substrate was annealed at 600°C for 10 minutes with ramping up and ramping down time 10 minutes to reach the desired temperature. The substrate with 2D materials flakes and devices was annealed at lower temperature (250°C for 30 minutes) to minimize the thermal treatment effects in 2D materials.

We adopted multiple transfer steps to stack the 2D materials for complex device structure. Every step in the transfer process is crucial which can easily introduce impurities from PDMS stamp and form wrinkles during transfer process. To remove impurities and wrinkles during transfer process, the substrate was annealed at 400°C for 30 minutes in every steps of transfer. The substrate was annealed at 250°C for 30 minutes after transfer of TMDs flakes to minimize the thermal defects in TMDs channel. Non-contact mode AFM was used to determine dimensions and cleanness of the sample. Transport properties of the FET devices were measured by a Keithley 4200 semiconductor parameter analyzer in a Lakeshore Cryogenic probe station under high vacuum (~ 1×10^{-6}Torr) and in a Physical Property Measurement System (PPMS) from Quantum Design.

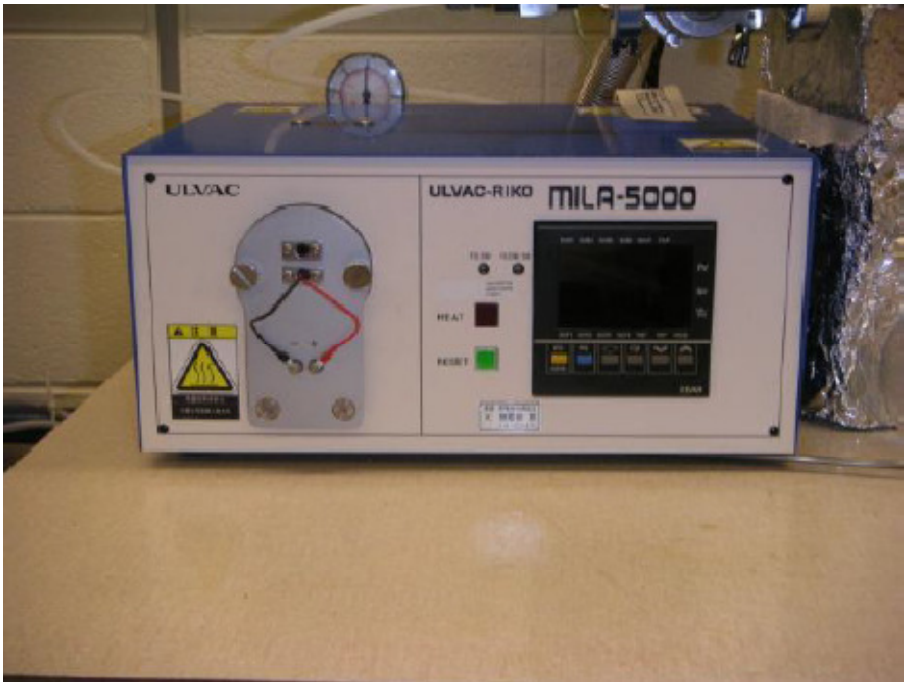

Fig.2.5.1 Ulvac mila-5000 annealing tool

2.6 KEITHLEY 4200 SEMICONDUCTOR PARAMETER ANALYSER

The device after defined Ti/Au electrodes is kept in Lakeshore cryogenic probe station chamber and pumps it overnight to reach the pressure down to ~$1x10^{-6}$torr. The Keithley 4200

parameter analyzer is used to characterize its electrical properties at different temperatures varying from 77K to 300K by using liquid nitrogen.

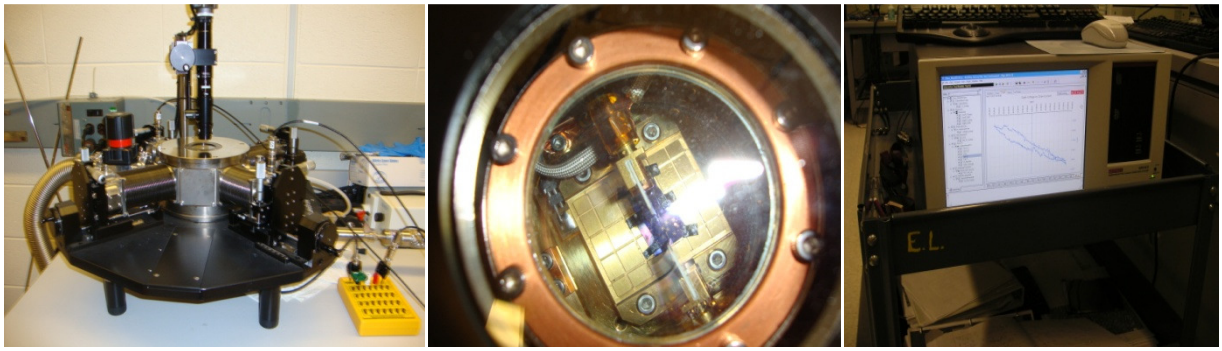

Fig.2.6.1 The cryogenic probe station, its top inner view and Keithley 4200 semiconductor parameter analyzer

2.7 PHYSICAL PROPERTY MEASUREMENT SYSTEM

The PPMS is used to measure transport properties of our sample in magnet field at room temperature down to cryogenic temperatures. The Quantum Design PPMS (Model 6000) used for characterizing our field effect transistors have the following specifications:

1. Magnetic Field Range: -9T to +9T

2. Temperature Range: 1.8-400 K

3. AC Frequency Range: 10 Hz to 10 kHz

4. AC Field Amplitude Range: 2 mOe to 15 Oe

5. Sensitivity of DC magnetization measurements: 2.5 x 10^{-5} emu

6. Sensitivity of AC susceptibility measurements: 2 x 10^{-8} emu

The physical property measurement system by quantum design is used to measure device transport properties at different temperature ranging from 4K to 300K in a helium cryogenic system. Magnetic field is applied in Hall bar configuration to perform Hall measurements for our Hall bar devices.

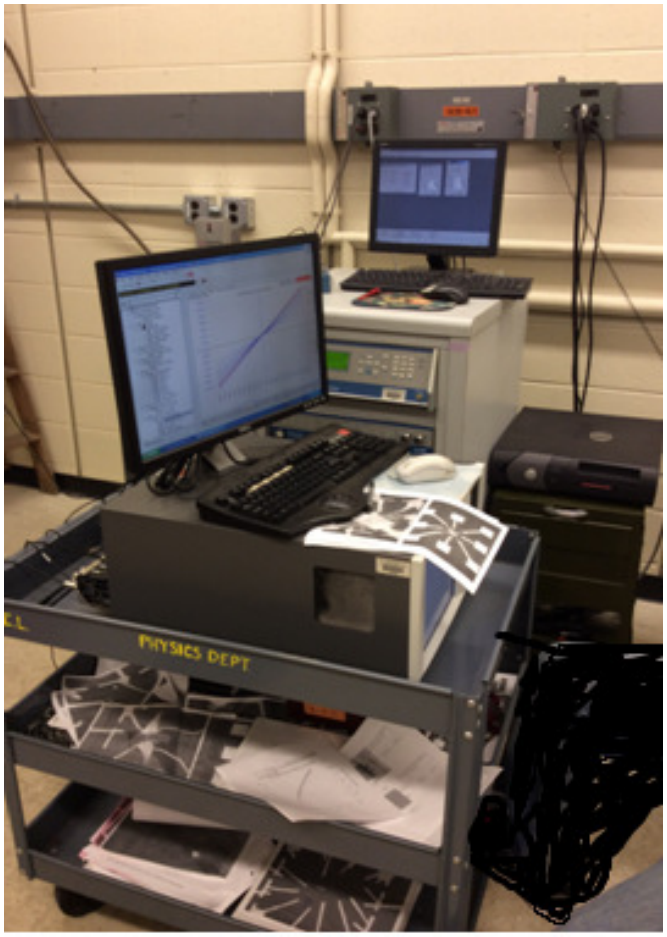

Fig.2.7.1 Physical Property Measurement System (PPMS) and Keithley 4200 semiconductor parameter analyzer

2.8 LCR METER

We used HP 4284A precision LCR meter for our measurements. HP 4284A precision LCR meter measures two components of the complex parameters at the same time of a measurement cycle. The primary measurement parameters are: absolute value of impedance (|Z|), absolute value of admittance (|Y|), inductance (L), capacitance (C), resistance (R), conductance (G) and the secondary measurement parameters are: dissipation factor (D), quality factor (Q), equivalent series resistance (R_S), equivalent parallel resistance (R_P), reactance (X), susceptance (B), phase angle (θ).

The HP 4284A precision LCR meter is used to measure the capacitance of the dielectric used to fabricate devices. It has frequency range from 20 Hz to 1 MHz with different mode of measurements. MIM junction is designed by sandwiching dielectric between two metal electrodes. Capacitance is measured with sweeping the bias voltage at different frequencies level by applying low AC system voltage (50 mV to 100mV). The capacitance is measured in C_p:D configuration to minimize the parasitic capacitance effects. To measure the capacitance more precisely, the recorded measure value is set at least average of 8 consecutive measurements.

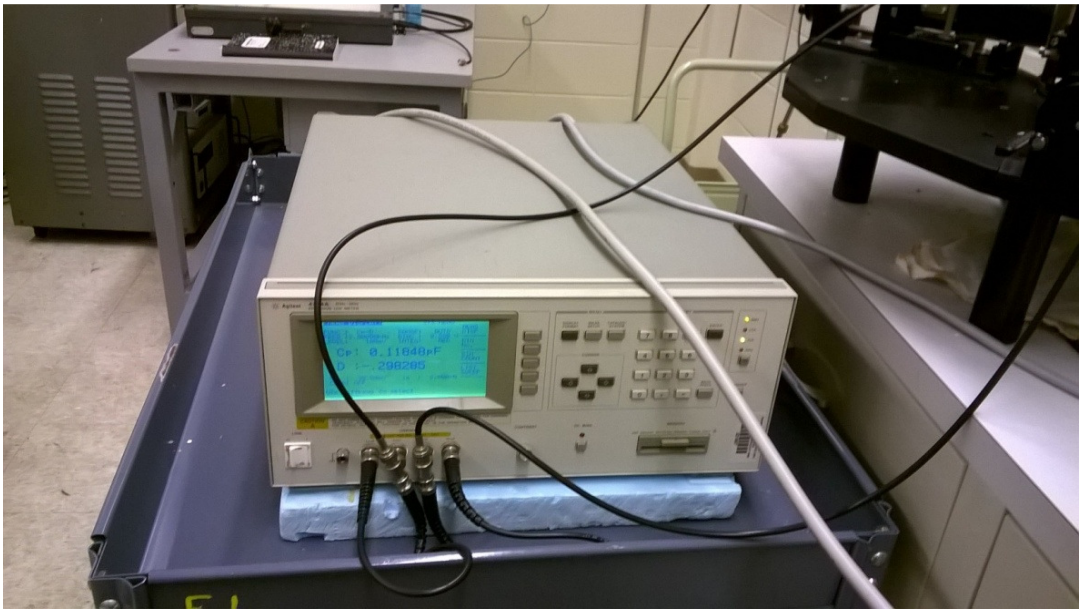

Fig.2.8.1 Alignment 4284A precision LCR meter

CHAPTER 3 STUDY OF INTRINSIC AND SUBSTRATE DEPENDENCE TRANSPOR TPROPERTIES OF MoS_2 FIELD EFFECT TRANSISTOR

3.1 INTRODUCTION

Two dimensional (2D) layered crystals have become one of the most attractive materials for future electronics and optoelectronics due to their unique properties. Graphene has shown extremely high charge-carrier mobility, optical transparency, and broadband absorption.[65-69] However, a zero band gap in grapheme limits its potential in digital and optical applications.[70, 71] Monolayer and multilayer metal dichalcogenides (TMDs) such asMoS_2, $MoSe_2$, WSe_2 and WS_2 have exhibited desirable "graphene like" properties including a reasonably high carrier mobility, mechanical flexibility, chemical and thermal stability.[5-19] Moreover, unlike grapheme they offer the advantage of a substantial band gap, which is needed for digital electronic applications. In addition, pristine surfaces of TMDs are free of dangling bonds, which reduces surface roughness scattering and interface traps. The properties of TMDs have made them stand out as two-dimensional materials beyond graphene for electronic and optoelectronic applications. As one of the most studied members of the TMD family, MoS_2 FETs have demonstrated promising device characteristics including a high ON/OFF ratio of $>10^8$ and a nearly ideal low subthreshold swing (SS) of ~ 70mV/dec.[3, 9]

In order to optimize the performance of MoS_2 FETs for electronic applications, it is essential to understand the dominant intrinsic and extrinsic scattering mechanisms that limit the carrier mobility, especially at room-temperature. However, the electron mobilities of monolayer and multilayer MoS_2 devices reported so far by multiple groups vary widely. Experimentally observed room-temperature mobility values of monolayer MoS_2 has been reported vary from less than 1 to ~ 80 $cm^2V^{-1}s^{-1}$,[7, 11, 12, 14, 72-74] which are significantly below than the theoretical limit of ~410 $cm^2V^{-1}s^{-1}$ when only the intrinsic phonon scattering is considered.[58] On the other hand,

multilayer MoS_2 devices have showed generally higher mobility values, depending on both their thicknesses and the substrate/dielectric used. While reported mobility values of multilayer MoS_2 transistors on conventional SiO_2 substrates are typically from less than 1 to ~ 60 $cm^2V^{-1}s^{-1}$ [13, 73, 75, 76], relatively high mobility values up to ~ 180 $cm^2V^{-1}s^{-1}$ and ~ 480 $cm^2V^{-1}s^{-1}$ were also reported for multilayer MoS_2 on SiO_2 and PMMA substrates, respectively.[77, 78] The large variation of experimentally observed MoS_2 mobilities strongly suggests that they were likely limited by extrinsic scattering mechanisms which may originate from MoS_2 channel such as sulfur vacancies, structural defects and native impurities as well as from the extrinsic environment such as the charged impurities and charge traps in the substrate and at the channel/substrate interface, substrate surface roughness, and substrate remote surface optical phonons. Hexagonal boron nitride (h-BN) is expected to be an ideal substrate material for minimizing the external scatterings because it has ultraclean and atomically flat surfaces without dangling bonds, free of charged impurities and charge traps, has a high optical phonon energy (~ 150 meV) that reduces phonon population at high temperature and minimizes surface phonon scattering at room temperature.[79] Record high Hall mobility over 30,000 cm^2/Vs has been reported on h-BN encapsulated few-layer MoS_2 at cryogenic temperatures recently, but the room temperature Hall mobility of the h-BN encapsulated MoS_2 devices did not show any obvious improvement over previously reported MoS_2 devices on SiO_2, Al_2O_3 and PMMA in spite of their extremely high mobilities at low temperatures.[80] So the open questions at present are: *what is the intrinsic limit of mobility in MoS_2 FETs* and *to what extent the mobility is affected by the extrinsic factors*.

So we study systematically MoS_2 intrinsic band mobility as a function of MoS_2 channel thickness, carrier density and temperature on four different types of substrates with varying dielectric constants, surface roughness, charged impurities and charge traps, surface chemistry

and surface polar optical phonon energy. In addition to commonly used SiO_2 and ultraclean h-BN substrates, we also chose SiO_2 modified by octadecyltrimethoxysilane (OTMS) self-assembled monolayer (SAMs), Al_2O_3 to study the substrate effects on transport properties of MoS_2 channel. OTMS modified SiO_2 substrate has been demonstrated to enhance the mobility in graphene devices in comparison withSiO_2substrate, which was attributed to the effective isolation of the graphene channel from the charged impurities at the SiO_2 surface by closely packed inert alkyl chains in the OTMS SAMs.[52] Al_2O_3 is a widely used high-κ dielectric material that is expected to more effectively screen charge impurities than SiO_2, and yet its lowest optical photon energy of 87 meV is higher than that of SiO_2 (~ 60 meV), which is expected to reduce surface phonon scattering.[81]On the other hand, hexagonal boron nitride (h-BN) is expected to have superior properties for minimizing the external scatterings because it has ultraclean and atomically flat surfaces without dangling bonds, is free of charged impurities and charge traps, and has a high optical phonon energy (~ 150 meV).[79] **Table 3.1.1** is a survey of mobility of $MoS_2$with different thicknesses reported in the literature by using different contact materials and different dielectric in back gate and top gate configurations at room temperature. The field effect mobility values of electrons vary from below 1 cm^2V^{-1} s^{-1} to over 200cm^2V^{-1} s^{-1} on SiO_2 substrate and up to 470 cm^2V^{-1} s^{-1} on PMMA.A close examination of the reported field-effect mobility and the Hall mobility reveals that the variation of former is significantly wider than the latter. The Hall mobility falls into a reasonably narrow range with weak dependences on the number of MoS_2 layers and contact materials. The fundamental question that arises is: what is the cause of the variations?

Contact	Thickness	Dielectric	μ at RT (cm^2V^{-1} s^{-1})	Reference
Au	1L	TG:Al_2O_3	80	X. Duan et. al. (Nat. Nanotechnol., 2014)
Ti	1L	TE:Si_3N_4	71.8	D. J. Late et. al. (ACS Nano, 2012)

Au	1L	BG:SiO_2	64	V. K. Sangwan et. al. (Nano Lett., 2013)
Au	1L	BG:SiO_2	59	D. Lembke et. al. (Nanoscale, 2015)
Ti	1L	BG:SiO_2	20 (Hall)	B. W. H. Baugher et. al. (Nano Lett., 2013)
Mo	1L	BG:Al_2O_3	11 - 13	J. Kang et. al. (Appl. Phys. Lett., 2014)
Ti	1L	BG:SiO_2	0.5	G.-H. Lee et. al. (ACS Nano, 2013)
Ti	1L	BG:BN	7.6 - 12	G.-H. Lee et. al. (ACS Nano, 2013)
Au	1L	BG:SiO_2	1	M. Y. Chan et. al. (Nanoscale,2013)
Ti	1L	BG:BN	10	M. Y. Chan et. al. (Nanoscale,2013)
Cr	1L	BG:SiO_2	1.1 - 10	D. J. Late et. al. (ACS Nano, 2012)
Cr	1L	Suspended	0.9	T. Jin et. al. (J. Appl. Phys.,2013)
Cr	1L	BG:SiO_2	0.1	T. Jin et. al. (J. Appl. Phys.,2013)
Cr	1L	Suspended	0.05	A. R. Klots et. al. (Sci. Rep.,2014)
Ti	2L	BG:SiO_2	80 (Hall)	B. W. H. Baugher et. al. (Nano Lett., 2013)
Ti	2L	BG:SiO_2	35	Y. Guo et. al. (ACS Nano, 2014)
Au	2L	BG:SiO_2	33	D. Lembke et. al. (Nanoscale, 2015)
Gr	1-6L	BG:BN	40 – 120(Hall)	X. Cui et.al. (Nat. Nanotechnol., 2014)
Au	2L	TG:Al_2O_3	27	X. Duan et. al. (Nat. Nanotechnol., 2014)
Ti	2L	BG:SiO_2	7	G.-H. Lee et. al. (ACS Nano, 2013)
Ti	2L	BG:BN	24	G.-H. Lee et. al. (ACS Nano, 2013)
Mo	2L	BG:Al_2O_3	11 - 14	J. Kang et. al. (Appl. Phys. Lett., 2014)
Au	2L	BG:SiO_2	3.5	M. Y. Chan et. al. (Nanoscale,2013)
Ti	2L	BG:SiO_2	4	H. Qiu et. al. (Appl. Phys.Lett., 2012)
Ti	2L	BG:SiO_2	0.12	H. Qiu et. al. (Appl. Phys.Lett., 2012)
Au	2-3L	BG:SiO_2	19	R. Kappera et. al. (Nat. Mater., 2014)
1T	2-3L	BG:SiO_2	46	R. Kappera et. al. (Nat. Mater., 2014)
Au	2-3L	TG:HfO_2	3.5	R. Kappera et. al. (Nat. Mater., 2014)
1T	2-3L	TG:HfO_2	12.5	R. Kappera et. al. (Nat. Mater., 2014)
Sc	2-3L	BG:SiO_2	26	S. Das et. al. (Nano Lett., 2013)
Au	3L	TG:IG	65 - 95	L. Chu et. al. (Sci. Rep., 2014)
Ti	3L	BG:SiO_2	9	G.-H. Lee et. al. (ACS Nano, 2013)
Ti	3L	BG:BN	45	G.-H. Lee et. al. (ACS Nano, 2013)
Au	3L	BG:SiO_2	36	D. Lembke et. al. (Nanoscale, 2015)
Ni	3L	TG:ZrO_2	25	H. Fang et. al. (Nano Lett., 2013)
Permallo y	3L	BG:SiO_2	27	W. Wang et. al. (Sci.Rep., 2014)
Ni	3L	TG:IG	12	J. Pu et. al. (Nano Lett., 2012)
Au	3L	TG:Al_2O_3	10	X. Duan et. al. (Nat. Nanotechnol., 2014)
Cr	3-5L	TG:Y_2O_3/HfO	47.7	X. Zou et. al. (Adv. Mater., 2014)

Ti	4L	BG:SiO_2	5	G.-H. Lee et. al. (ACS Nano, 2013)
Mo	5L	BG:Al_2O_3	25-26	J. Kang et. al. (Appl. Phys. Lett., 2014)
Ti	5L	BG:SiO_2	15	G.-H. Lee et. al. (ACS Nano, 2013)
Ti	5L	BG:SiO_2	5	M. M. Perera et. al. (ACS Nano, 2013)
Au	6L	BG:SiO_2	49	Y. Guo et. al. (ACS Nano, 2014)
Ti	6L	BG:SiO_2	42	Y. Guo et. al. (ACS Nano, 2014)
Au	7L	BG:SiO_2	75	M. M. Perera et. al. (ACS Nano, 2013)
Ni or Au	7L	BG:SiO_2	28	H. Liu et. al. (ACS Nano, 2012)
Ni	5-6L	BG:SiO_2	24	A. T. Neal et. al. (ACS Nano, 2013)
Ti	8nm	BG:SiO_2	40	M. M. Perera et. al. (ACS Nano, 2013)
Sc	10nm	BG:SiO_2	184	S. Das et. al. (Nano Lett., 2013)
Ti	10nm	BG:SiO_2	125	S. Das et. al. (Nano Lett., 2013)
Ni	10nm	BG:SiO_2	36	S. Das et. al. (Nano Lett., 2013)
Pt	10nm	BG:SiO_2	21	S. Das et. al. (Nano Lett., 2013)
BLG	10nm	TG:BN	26 - 33	T. Roy et. al. (ACS Nano, 2014)
Ti	11nm	BG:SiO_2	8.4	J. Na et. al. (Nanoscale, 2014)
Ti	11nm	TG:Al_2O_3	9.8	J. Na et. al. (Nanoscale, 2014)
Cr	1-17nm	Suspended	0.01 - 46	F. Wang et. al. (Nanotechnology,2015)
Cr	1-17nm	Suspended	0.5 - 105	F. Wang et. al. (Nanotechnology,2015)
Ti	12nm	BG:SiO_2	150	N. R. Pradhan et. al. (Appl. Phys. Lett.,2013)
Ti	12nm	BG:SiO_2	91	N. R. Pradhan et. al. (Appl. Phys. Lett.,2013)
Co	13nm	BG:SiO_2	12	A. Dankert et. al. (ACS Nano, 2014)
1nm TiO_2	13nm	BG:SiO_2	76	A. Dankert et. al. (ACS Nano, 2014)
Ti	50nm	BG:PMMA	470	W. Bao et. al. (Appl. Phys. Lett., 2013)
Ti	15-19nm	BG:SiO_2	30-60	W. Bao et. al. (Appl. Phys. Lett., 2013)

Table 3.1.1 A survey of mobilities of different thickness MoS_2 reported in literature by using different contact materials and different dielectric in back gate and top gate configurations. Permalloy is a soft magnetic alloy of nickel (80%) and iron (20%).

3.2 EXPERIMENTAL DETAILS

Thin MoS_2 flakes were produced from the MoS_2 bulk crystal supplied by SPI by a repeated splitting of bulk crystals using a mechanical cleavage method using adhesive blue tape and subsequently transferred to four different types of pre-cleaned substrates: SiO_2, SiO_2 modified by OTMS SAM, Al_2O_3 and h-BN. The transfer techniques on different substrates are as described below:

3.2.1 TRANSFER MoS_2 THIN FLAKES ON SiO_2 SUBSTRATE

Thin MoS_2 flakes were produced by a repeated splitting of bulk crystals using a mechanical cleavage method on adhesive tape. Conventional Si/SiO_2 substrate with 290 nm thermally grown SiO_2 layer on degenerately doped Si was cleaned by sonication in acetone and isoproponal (IPA). Plasma treatment and UV treatment were done to further clean the surface of the substrates. Thin flakes of MoS_2 produced by repeated slitting were transferred from adhesive tape to the pre-cleaned Si/SiO_2 substrates. Optical microscopy was used to identify thin MoS_2 flakes below 15 nm of thickness range on Si/SiO_2 substrate, which were further characterized by non-contact mode atomic force microscope (AFM).

3.2.2 TRANSFER MoS_2 THIN FLAKES ON SiO_2 SUBSTRATE MODIFIED BY OTMS SAM

A highly p-doped silicon substrate with 290 nm of thermally grown SiO_2 was clean by sonication in acetone and isoproponal (IPA) and treated by oxygen plasma for 10 min to enhance hydrophilicity. A 3mM octadecyltrimethoxysilane (OTMS) (supplied by Sigma– Aldrich) solution in trichloroethylene (TCE) was drop-casted on the entire substrate and allowed to assemble for 10s.The substrate was spun at 3000 rpm for 10 s to cover entire surface by OTMS and rested 10 seconds to dry the OTMS coated surface. The substrate was bath in ammonia (NH_3) vapor at room temperature overnight by keeping inside the well covered beaker containing NH_4OH separately in the small open vessel inside the beaker. Finally, the substrate was rinsed with de-ionized (DI) water and sonicated in toluene about 5 minutes. The OTMS forms self-assemble monolayer (SAM) on the SiO_2 surface which can be tested by the hydrophobic behavior of the surface. The thin layer of SAM is expected to be its thickness less than a nanometer. Thin flakes of MoS_2 were prepared on the scotch tape by mechanical cleavage method from its bulk crystal and transferred to the substrate modified by the OTMS SAM. The

substrate was observed under optical microscope to find thin MoS_2 flakes and non-contact mode atomic force microscope (AFM) was used to characterize them.

3.2.3 TRANSFER MoS_2 THIN FLAKES ON Al_2O_3 SUBSTRATE

A highly p-doped silicon substrate with 290 nm of thermally grown SiO_2 was clean by acetone and isoproponal (IPA) and treated by oxygen plasma for 10 min. A 60 nm of Al_2O_3 was deposited on the Si/SiO_2 substrate by chemical vapor deposition (CVD) method. The Si/SiO_2 substrate with Al_2O_3 capping layer was introduced into scotch tape having thin flakes of MoS_2 and transferred thin flakes on it. Optical microscopy and atomic force microscopy were used to identify the thin MoS_2 flakes and further characterized them.

3.2.4 TRANSFER MoS_2 THIN FLAKES ON h-BN SUBSTRATE

Thin h-BN flakes were produced by a repeated splitting of bulk crystals using a mechanical cleavage method on adhesive tape. Large, thin (~7 - 40 nm)and smooth surface h-BN was transferred on pre-cleaned Si/SiO_2 substrate. The h-BN flake surface was characterized by non contact mode AFM to ensure it is ultraclean and smooth. Poly-dimethylsiloxane (PDMS) gel was spin casted on silicon wafer at 400rpm for 30sec and kept on hot plate at 80℃ until 30 minutes and allowed to cool it down. The PDMS layer was cut it small pieces and gently transferred to scotch tape having thin flakes of MoS_2. The PDMS stamp was gently pressed and transferred to clean glass slide. The glass slide was kept under optical microscope and search for thin and clean MoS_2 flakes. Selected ultraclean and thin MoS_2 samples were transferred to the target ultraclean h-BN flakes by home-built precision transfer stage. Every step in the transfer process is crucial which can easily introduce impurities from PDMS stamp and form wrinkles during transfer process. To remove impurities and wrinkles during transfer process, the substrate was annealed at 400℃ for 30 minutes after every transfer steps were done. The substrate was

annealed at relatively low annealing temperature 250℃ for 30 minutes after transfer of MoS_2 flakes. The reason to anneal low annealing temperature after transfer MoS_2 flakes is to minimize the possibility of thermal defects in MoS_2 channel due to annealing. Non-contact mode AFM was used to determine dimensions, surface roughness and cleanness of the MoS_2sample.To minimize the influence by subtle variations in the material quality, MoS_2 devices on all four substrates were fabricated from a common MoS_2 bulk crystal.

We chose 3 - 14 nm thick MoS_2, because multilayer MoS_2 offers the advantages of lower contact resistance and higher drive current than monolayer MoS_2 due to its smaller band gap and higher density of states.[82] MoS_2 FET devices were fabricated using standard electron beam lithography and electron beam deposition of 5 nm of Ti and 40 nm of Au. We patterned additional voltage probes in between drain and source electrodes for four-terminal measurements to eliminate contact resistance contributions as shown in **Fig.3.3.1**. To directly measure the carrier density and Hall mobility, Hall bar devices are also fabricated. Optical images of typical MoS_2 Hall bar devices are shown in **Fig.3.3.10**. Electrical properties of the devices were measured by a Keithley 4200 semiconductor parameter analyzer in a Lakeshore Cryogenic probe station under high vacuum (~ 1×10^{-6}Torr) and in a Physical Property Measurement System (PPMS) from Quantum Design. To examine the quality of electrical contacts for low-temperature electrical measurements, we measured two-probe current-voltage characteristics on the MoS_2 devices at different temperatures and gate voltages.

3.3 RESULTS AND DISCUSSION

Four terminal MoS_2 FETs were fabricated on four different substrates as mentioned in experimental details section 3.2. AFM images of typical MoS_2 four probe devices are shown in **Fig.3.3.1**.To examine the quality of electrical metal contacts for electrical measurements; we

measured two-probe current-voltage characteristics on the MoS_2 devices at different temperatures and gate voltages. **Fig.3.3.3** and **Fig.3.3.4** show typical output characteristics (I_{ds} - V_{ds}) for MoS_2 FET devices on four different substrates, as mention in figure, measured at room temperature and 77 K, respectively. The I_{ds} - V_{ds} curves are linear at higher gate voltages (V_{bg}> 0 V at RT and V_{bg}> 40 V at 77 K) and the current at a given bias and gate voltages increases with decreasing temperature indicating nearly Ohmic contacts with negligible Schottky barrier.

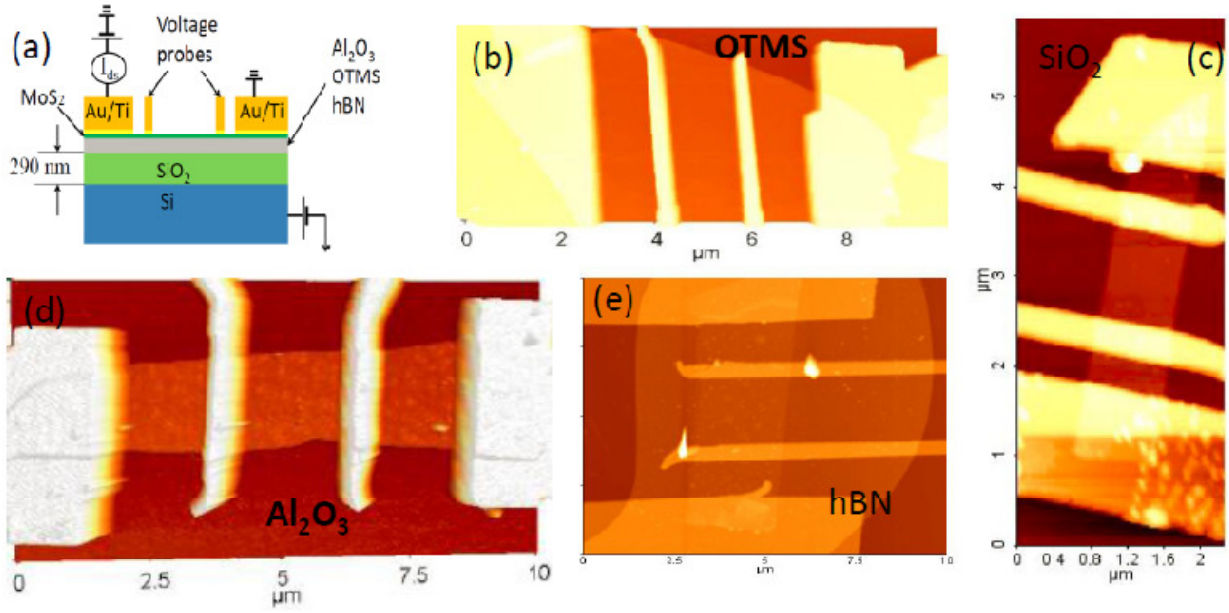

Fig.3.3.1 (a) Schematic diagram of MoS_2 FET on different dielectric substrates. AFM image of MoS_2 devices on (b) OTMS SAM (c) silicon dioxide (d) aluminum oxide (e) hexagonal boron nitride

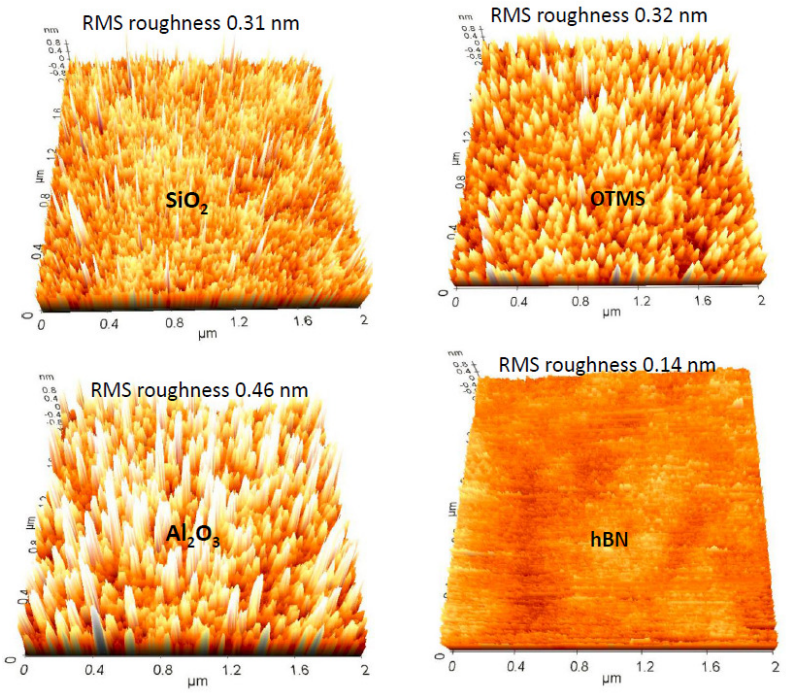

Fig.3.3.2 AFM image of surface roughness of (a) silicon dioxide (b) OTMS SAM (c) aluminum oxide (d) hexagonal boron nitride

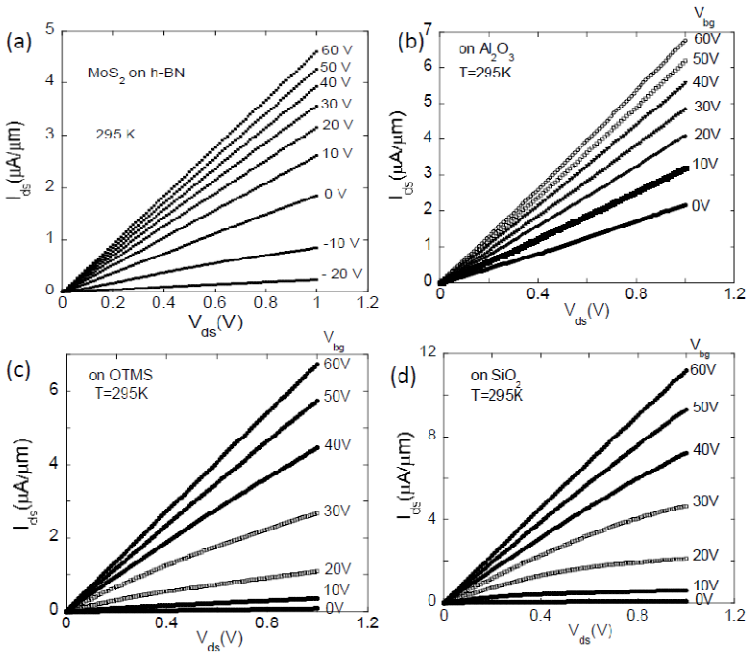

Fig.3.3.3 Room temperature output characteristics of MoS_2 FET on (a) hexagonal boron nitride (b) aluminum oxide (c) OTMS SAM (d) silicon dioxide

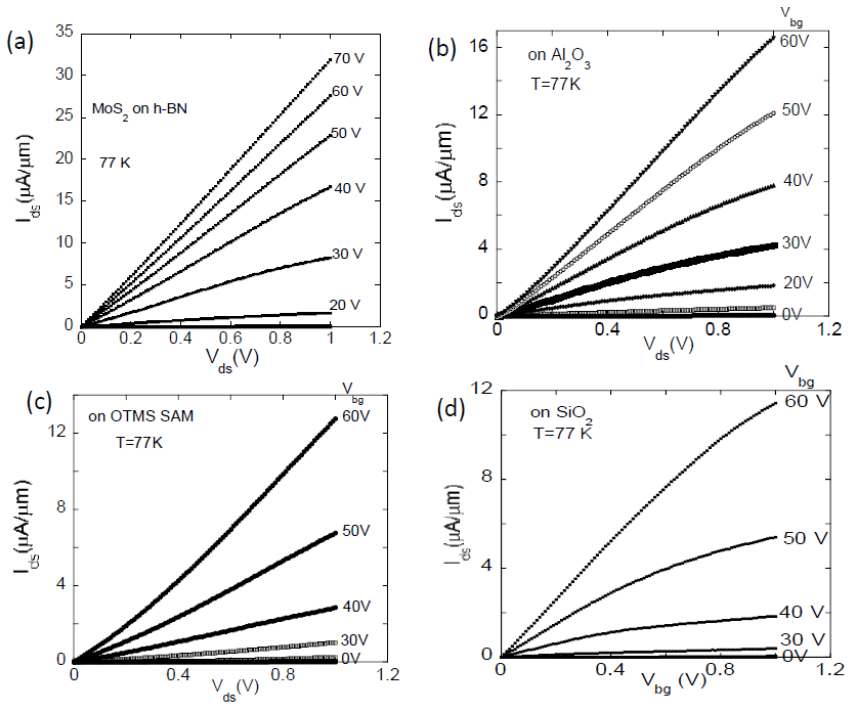

Fig.3.3.4 Output characteristics of MoS_2 FET at 77K on (a) hexagonal boron nitride (b) aluminum oxide (c) OTMS SAM (d) silicon dioxide

We now turn to exploring the substrate effects on the carrier mobility in few-layer MoS_2 FETs. We measure temperature dependence drain source current by sweeping gate voltage and calculate field-effect mobility from the channel conductivity as a function of gate voltage measured. Here the channel conductivity is defined as$\sigma = I_{\mathrm{ds}} \times \frac{L}{W} / V_{\mathrm{xx}}$, where L and W are the separation between two voltage probes and sample width respectively; and V_{xx} is the measured longitudinal voltage difference with applied drain source voltage V_{ds}= 50mV.**Fig.3.3.6 (a)** and **Fig.3.3.5** show typical room-temperature and temperature dependence channel conductivity(σ) as a function of gate voltage for four representative MoS_2 devices fabricated on four different types of substrates respectively. The back gate dependence conductivity curves show*n*-type behavior with two distinct nearly linear regions of different slopes, yielding higher field-effect mobility in the lower V_{bg} region than in the higher V_{bg} region. The field-effect mobility is calculated using the expression,

$$\mu_{FE} = 1/C_{bg} \times d\sigma/dV_{bg}$$

where C_{bg} is the geometric back-gate capacitance per unit area of the gate dielectric. The capacitance for MoS_2 devices on bare and OTMS-modified SiO_2 substrates is determined to be 1.20×10^{-8} F cm^{-2} for 290 nm of SiO_2 or 1.26×10^{-8} F cm^{-2} for285 nm of SiO_2 ($C_{bg} = 3.9 \times \varepsilon_0/290$ nm and the contribution of the OTMS atomic layer is negligible). The back-gate capacitance of the MoS_2 devices on Al_2O_3 and h-BN substrates is modeled as a dielectric stack consisting of Al_2O_3 or h-BN in series with SiO_2. [83] The gate dependence of room-temperature field-effect mobility exhibits two common features that are independent of substrate: *i*) a maximum (peak) value at intermediate carrier densities (~1- 3×10^{12} cm^{-2}), and *ii*) asymptotic approach to a nearly constant value at high carrier densities (>7×10^{12} cm^{-2})as shown **Fig.3.3.6 (b)**. To eliminate the possibility of random sample-to-sample variations and further investigate the thickness dependence of the mobility, we systematically measured multiple MoS_2 devices on SiO_2, OTMS-modified SiO_2, Al_2O_3, and h-BN. Saturation values of the field-effect mobility lies between ~ 40 cm^{2}V^{-1}s^{-1}to ~ 60 cm^{2}V^{-1}s^{-1}and peak values of the field-effect mobility fluctuates from ~60 cm^{2}V^{-1}s^{-1} to over 130 cm^{2}V^{-1}s^{-1} without clear showing thickness dependence. Although the field-effect mobility has been widely used to characterize the performance of MoS_2 and other TMDs as channel materials for FETs, it is also recognized that the field-effect mobility may differ significantly from the true carrier mobility (drift mobility) if the drift mobility changes with carrier density as,

$$\mu_{EF} = \mu + n\frac{d\mu}{dn}$$

In order for the four-terminal field-effect mobility to coincide with the true drift mobility, two conditions need to be met: *i*) the drift mobility is independent of carrier density, and *ii*) the change of carrier density with the gate voltage follows the relation, $\Delta n = C_{bg}\Delta V_{bg}$.

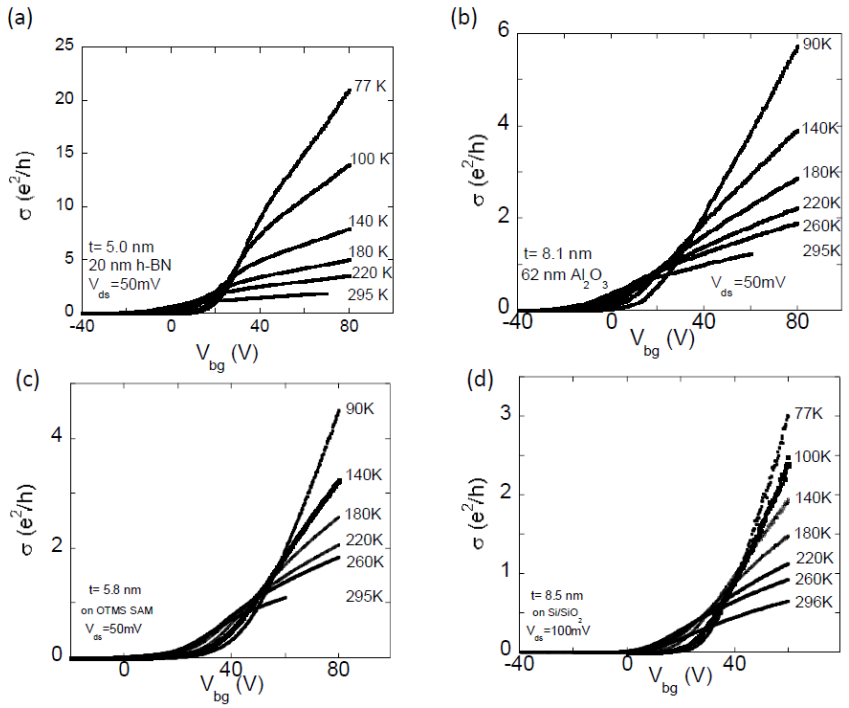

Fig.3.3.5 Temperature dependence conductivity (e^2/h) vs V_{bg} of MoS_2 FET on (a) hexagonal boron nitride (b) aluminum oxide (c) OTMS SAM (d) silicon dioxide

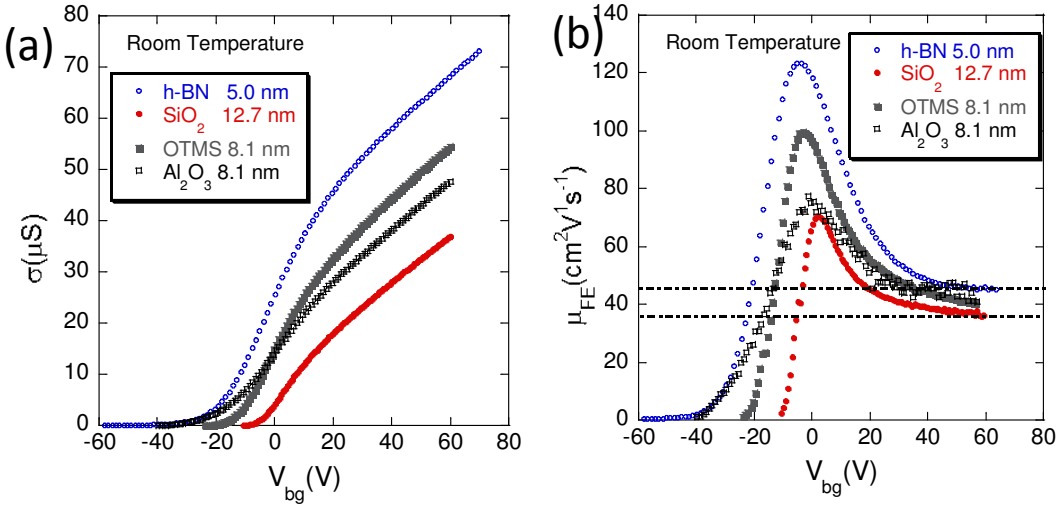

Fig.3.3.6 (a) Room temperature (295K) conductivity vs V_{bg} of MoS_2 FET on different substrates (b) Back gate dependence field effect mobility of MoS_2 FET on different substrates at room temperature

The equations to calculate to Hall mobility:

$$\text{Transverse resistance } (\boldsymbol{R_{xy}}) = \boldsymbol{V_{xy}/I_{ds}}$$

Hall resistance $(\boldsymbol{R_H}) = \frac{\boldsymbol{dR_{xy}}}{\boldsymbol{dB}}$

Carrier concentration $(\boldsymbol{n}) = \frac{\boldsymbol{1}}{\boldsymbol{eR_H}}$

Hall mobility $(\boldsymbol{\mu_H}) = \frac{\boldsymbol{\sigma}}{\boldsymbol{ne}}$

To more accurately determine the carrier mobility in our MoS_2 devices, we compare the field-effect mobility with the Hall mobility as a function of gate voltage. The Hall mobility μ_H is derived from $\mu_{\boldsymbol{H}} = \frac{\boldsymbol{\sigma}}{\boldsymbol{ne}}$, where σ is the four-terminal conductivity, *e* is the electron charge, and *n* is the sheet carrier density directly extracted from the Hall effect measurement: $\boldsymbol{n} = \frac{\boldsymbol{1}}{\boldsymbol{eR_H}}$. The Hall coefficient R_H is obtained from the magnetic-field dependence of the Hall resistance $\boldsymbol{R_H} = \frac{\boldsymbol{dR_{xy}}}{\boldsymbol{dB}}$; $and\ \boldsymbol{R_{xy}} = \boldsymbol{V_{xy}/I_{ds}}$, where V_{xy} is the transverse voltage measured along the sample width direction. **Fig. 3.3.11 (b)** and **(d)** displays both the four-terminal field-effect mobility and Hall mobility as a function of gate voltage measured at different temperature of MoS_2 FET on SiO_2 substrate. In contrast to the field-effect mobility, no obvious peak is observed in the gate dependence of Hall mobility which can be attributed to the reduced carrier localization and enhanced screening of Coulomb impurities with increasing carrier density with additional remote optical phonon from SiO_2 substrate, consistent with the results of Ye *et al.* [76] At sufficiently high carrier densities, the charge carriers are fully delocalized and the potential of charged impurities is fully screened by the gate induced carriers in the channel, leading to the saturation of Hall mobility. The discrepancy between the field-effect and Hall mobilities at relatively low gate voltages can be partially explained by the positive correlation between the Hall mobility and gate voltage. As a result, the field-effect mobility overestimates the true drift mobility by[12],

$$\mu_{EF} = \mu_H + \boldsymbol{n}\frac{\boldsymbol{d}\mu_H}{\boldsymbol{C_{bg}dV_{bg}}}$$

Interestingly, the field-effect and Hall mobilities quantitatively agree with each other at high carrier densities. It is worth noting that carrier density determined by the Hall effect may overestimate the true carrier density by a Hall factor (usually between 1 and 2), and thus may underestimate the true drift mobility.[76] To further verify that the nearly gate-independent Hall and field-effect mobilities at high carrier densities are indeed the true drift mobility, we plot the carrier density extracted from the Hall effect measurement as a function of gate voltage in **Fig. 3.3.11 (c)**. **Fig. 3.3.11 (c)** shows the carrier density linearly depends on the back gate voltage, $\boldsymbol{\Delta n = C_{bg}\Delta V_{bg}}$**.** The slope in the higher carrier density region corresponds to a Hall capacitance of $C_H = \frac{dn}{dV_{bg}}e$ ~1.21 $\times 10^{-8}$ F cm^{-2}, in good agreement with the geometric capacitance C_{bg}. In contrast, the slope back gate dependence carrier density at high temperature is deviates from that slope at lower temperatures. Here, the carrier density dependence of the slope cannot be explained by the Hall factor. Possible causes of C_H enhancement at high temperature include thermal activation of charge carriers and reduced localization with increasing carrier density.

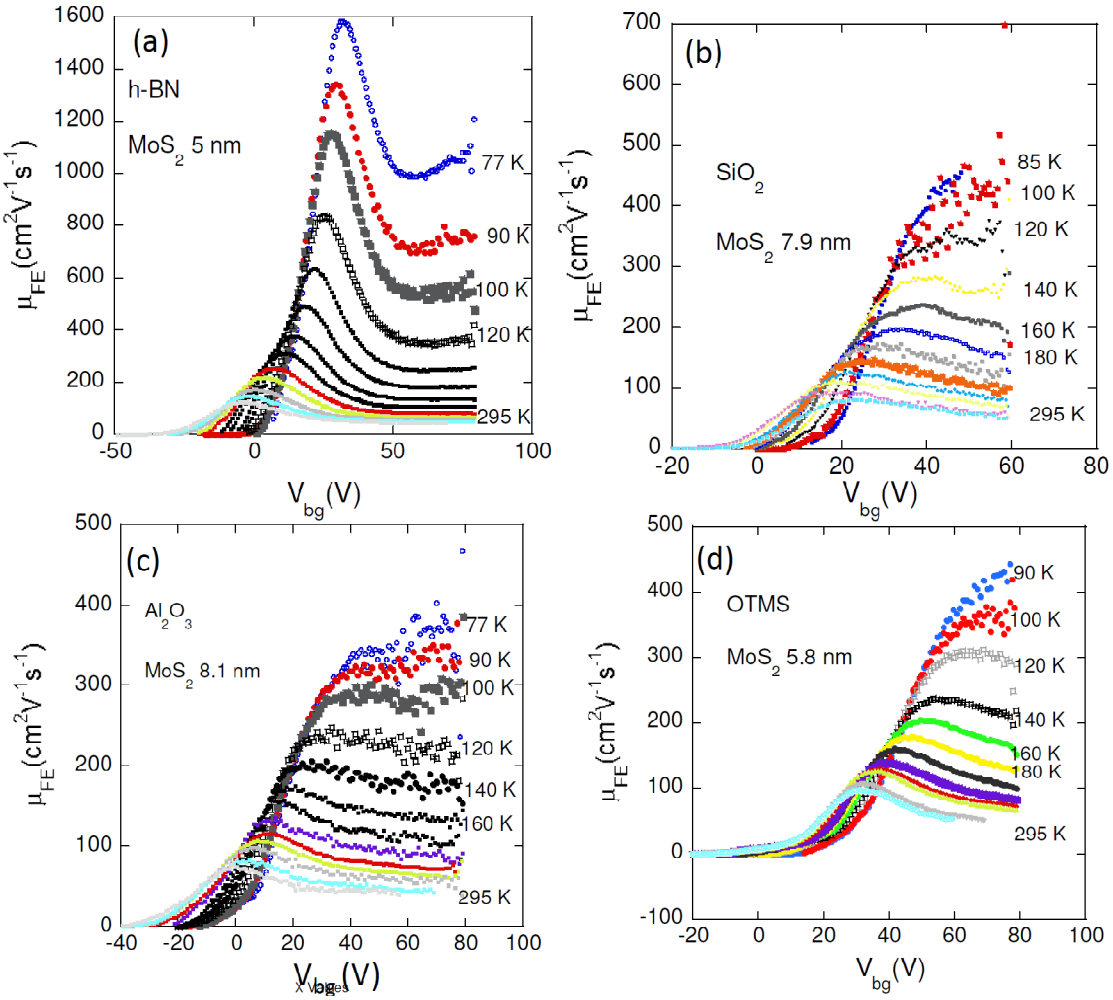

Fig.3.3.7 Back gate dependence field effect mobility of MoS_2 FET at different temperatures on (a) h-BN (b) SiO_2 (c) Al_2O_3 (d) OTMS SAM treated SiO_2

To further elucidate the origin of the observed gate dependence of field-effect mobility and carrier density as well as the scattering mechanisms in the MoS_2 channel, we measured the four-terminal conductivity as a function of gate voltage of MoS_2 devices on different substrates at various temperatures. **Fig. 3.3.5** shows the temperature dependence of four-terminal conductivity as a function of back-gate voltage of MoS_2 devices on four different substrates. In all devices, with increasing electron density we observe a crossover form insulating regime, where the conductivity increases with increasing temperature, to a metallic regime, where the

conductivity decreases with temperature. This crossover occurs near the critical conductivity of e^2/h, consistent with previously reported metal-insulator transition (MIT) in MoS_2 and other TMDs.[11] In the insulating region, where the Fermi level lies in the localized states below the mobility edge, the conductivity is largely determined by conducting electrons thermally excited to the extended states above the mobility edge, which increases exponentially with temperature. As the Fermi level moves closer to the mobility edge with increasing gate voltage, the thermal activation barrier decreases, leading to a rapid increase of the density of conducting electrons in the extended states. As a result, the density of conducting electrons increases faster than $C_{bg}\Delta V_{bg}$. In conjunction with the gate dependence of the field-effect mobility, this can lead to a field-effect mobility peak. After the Fermi level is moved above the mobility edge with further increasing the gate voltage, the conductivity is dominated by the transport of conducting electrons in the extended states primarily induced by the gate voltage ($\Delta n = C_{bg}\Delta V_{bg}$, $where C_{bg} = C_H$). Consequently, the temperature dependence of conductivity is dominated by the temperature dependence of electron mobility in the extended states (or conduction band mobility), leading to band transport or metallic behavior. Therefore, the field-effect mobility of MoS_2 devices in this high density metallic region represents the true drift mobility, while it overestimates the mobility at lower carrier densities.[58]

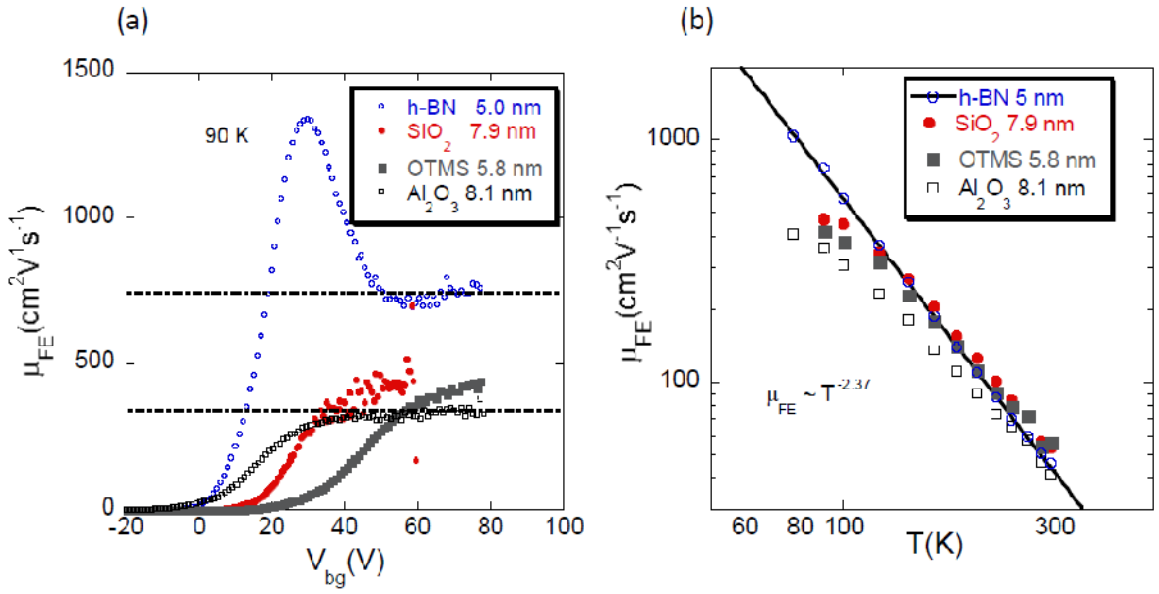

Fig.3.3.8 (a) Back gate dependence field effect mobility of MoS_2 FET on different substrates at 77K (b) Temperature dependence field effect mobility of MoS_2 FETs on different substrates

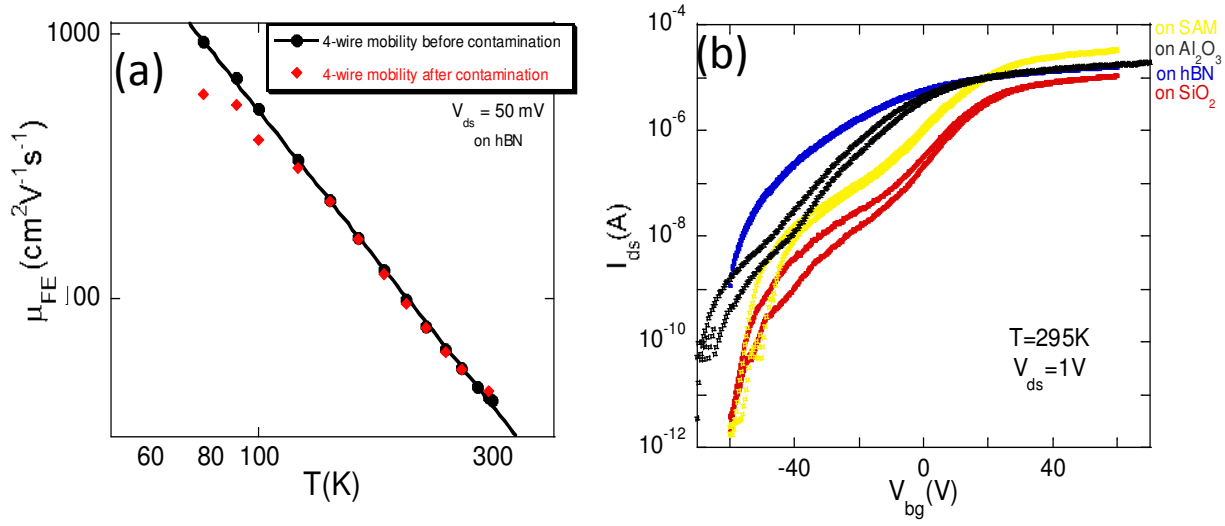

Fig.3.3.9 (a) Temperature dependence field effect mobility of MoS_2 FETs on h-BN before contamination (black circle) & after contamination (red square) (b) comparison of hysteresis of MoS_2 FETs on different substrates

To further explore the effects of substrate on the carrier mobility and shed light on the scattering mechanisms limiting the electron mobility of MoS_2, we investigate the temperature dependence of the drift mobility (field-effect mobility at high carrier densities) in MoS_2 samples on all four different types of substrates. **Fig. 3.3.8 (a)** shows the field-effect mobility as a

function of gate voltage at 90 K for the MoS_2 devices exhibited in **Fig.3.3.1**. While the peak in the field-effect mobility as a function of gate voltage for the device on h-BN is preserved, the field-effect mobility of MoS_2 devices on other substrates increases monotonically with gate voltage at low temperatures. Furthermore, the field-mobility in the high carrier-density plateau region is nearly twice as large in MoS_2 on h-BN than on other three substrates. The lack of a peak in the gate dependence of field-effect mobility and substantially smaller mobility at high carrier densities on SiO_2 (with or without OTMS modification) and Al_2O_3 strongly suggests that these substrates introduce additional disorder that induces carrier localization and degrades mobility at relatively low carrier densities that are inadequate to screen the potential of charge impurities. **Fig.3.3.8 (b)** shows the temperature dependence of drift mobility of representative MoS_2 devices on four different types of substrates. The mobility values of a 5 nm thick MoS_2 devices on h-BN follows $\mu \sim T^{-\gamma}$ dependence with $\gamma \approx 2.4$ for the entire temperature range between 77 and 295 K. This is consistent with the theoretically calculated phonon-limited mobility in MoS_2, which follows $\mu \sim T^{-\gamma}$ dependence where the exponent γ depends on the dominant phonon scattering mechanism with ~ 2.6 in bulk MoS_2 and lower for carriers in monolayer MoS_2.[58, 84] The exponent $\gamma = 2.4$ observed in our MoS_2 on h-BN is also in good agreement with the γ values recently reported on h-BN encapsulated mono- and few-layer MoS_2 with graphene contacts, further indicating that the mobility in our MoS_2 devices approaches the phonon-limited mobility.[85] In contrast, the field-effect mobility of the MoS_2 devices on SiO_2 (with and without OTMS) and Al_2O_3 substrates exhibits a clear downward deviation from the power-law behavior at low temperature region. At 90 K, the field-effect mobility values of the devices on SiO_2, OTMS modified SiO_2 and Al_2O_3 are 460 $cm^2V^{-1}s^{-1}$, 430 $cm^2V^{-1}s^{-1}$, and 350 $cm^2V^{-1}s^{-1}$, respectively, which are much smaller than the mobility of the MoS_2 device on h-BN

(760 $cm^2V^{-1}s^{-1}$). The significant substrate dependence of carrier mobility observed at low temperatures indicates that extrinsic scattering mechanisms originating from the substrate or substrate/channel interface further limit the mobility at low temperatures.

To understand the substrate effects on the mobility of MoS_2 at low temperaturs, we consider various mobility-limiting scattering mechanisms as formulated by Mathiessen's rule,

$$\boldsymbol{\mu^{-1} = \mu_{INT}^{-1} + \mu_{SD}^{-1} + \mu_{CI}^{-1} + \mu_{SR}^{-1} + \mu_{SPP}^{-1}}$$

Here μ_{INT}^{-1} represents the mobility limited by intrinsic scattering from lattice phonons, μ_{SD}^{-1} presents mobility limited by structural defects, and μ_{CI}^{-1}, μ_{SR}^{-1} and μ_{SPP}^{-1} represent mobility limited by extrinsic scattering from Coulomb impurities (CI), the surface roughness (SR), and the dielectric surface polar optical phonons (SPP), respectively. The intrinsic mobility $\mu_{INT}$and mobility limited by structural defects μ_{SD} are expected to be similar for MoS_2 FETs on all substrates, since all our devices are fabricated from the same MoS_2 crystal. We exclude SR as a main scattering mechanism due to its extremely strong power-law dependence on the sample thickness ($\mu_{SR} \sim t^6$), which is not observed in our devices.[82] Interfacial Coulomb impurities are expected to play an increasingly important role in determining the mobility of MoS_2 devices on SiO_2 substrates as temperature and carrier density decrease. The μ_{CI} increases with increasing carrier density (gate voltage) due to enhanced screening of Coulomb potential, and decreases with the decreasing distance between charge carriers and CIs. However, the former is expected to be a stronger effect than the latter because nearly all carriers are already confined within nanometer range of the MoS_2/substrate interface in our MoS_2 devices when they are electrically gated.[82] As a result, μ_{CI} should increase with increasing carrier density.

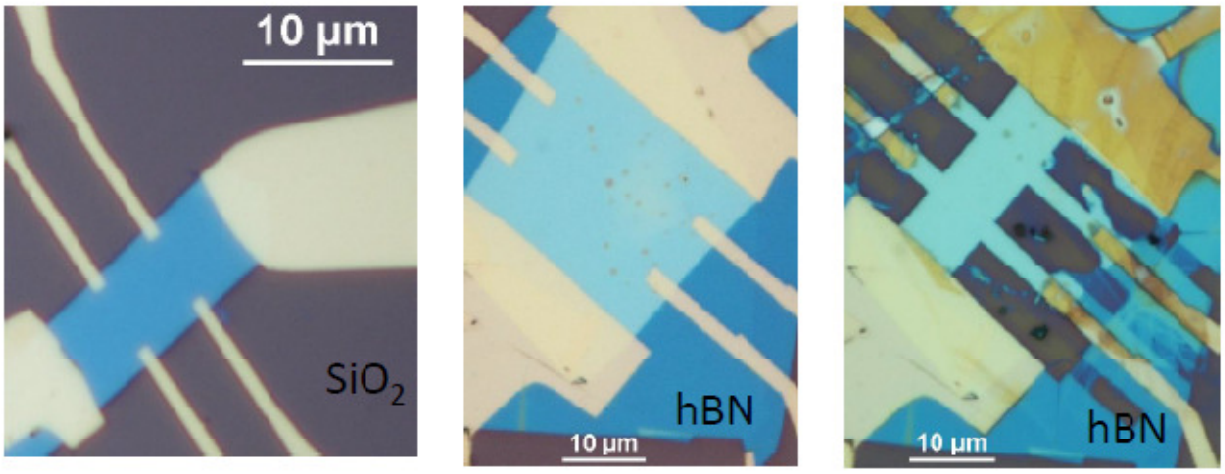

Fig.3.3.10 Hall bar devices, on SiO_2, on h-BN and after etching with hall bar on h-BN (to study the evasive effect of inner gold electrodes)

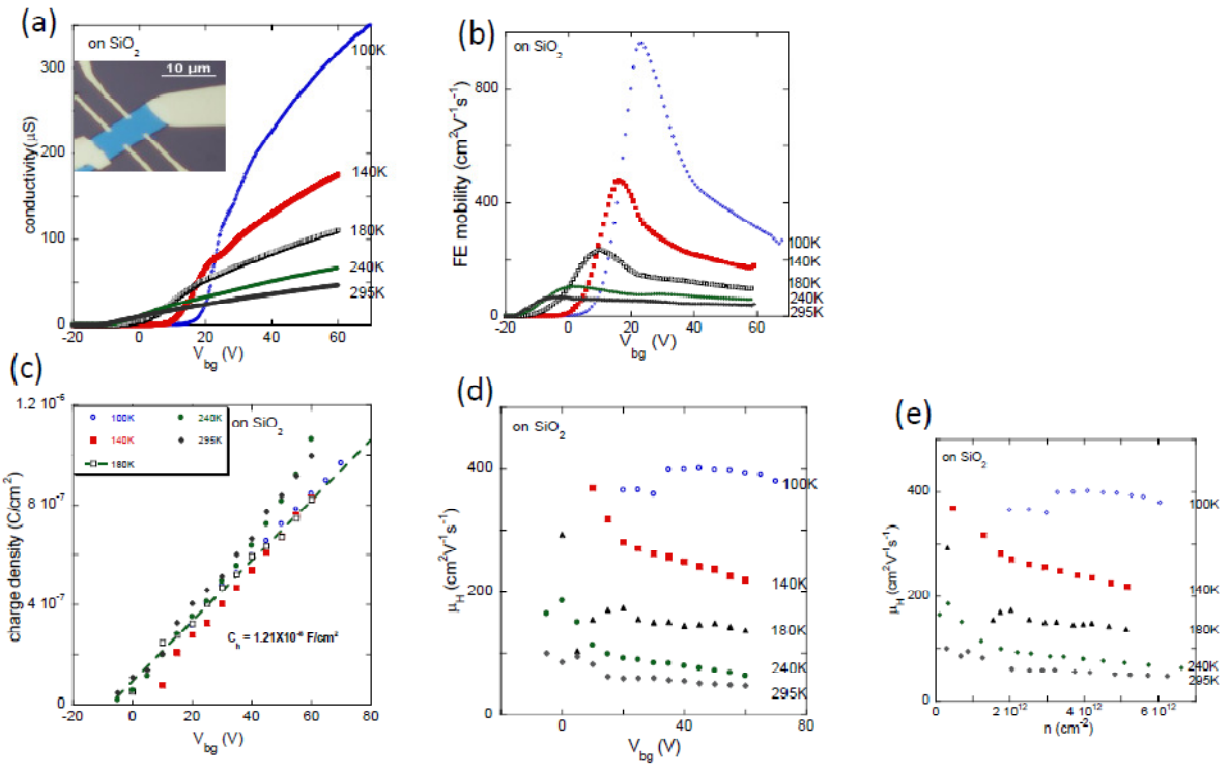

Fig.3.3.11 Gate dependence four (a) probe conductivity (b) four probe field effect mobility (c) charge carrier density and (d) hall mobility at different temperatures on SiO_2 and hall bar device on SiO_2 (in inset (a)) (e)carrier concentration dependence hall mobility at different temperatures on SiO_2

Next, we consider the effects of surface roughness scattering on the mobility of our MoS_2 devices. **Fig.3.3.2** shows AFM topographic images acquired in the vicinity of MoS_2 samples on SiO_2, OTMS-modified SiO_2, Al_2O_3 and h-BN, from which the RMS surface roughness is determined to be 0.31 nm, 0.32 nm, 0.46 nm and 0.14 nm, respectively. The reduced low-temperature mobility in MoS_2 devices on SiO_2, OTMS modified SiO_2 and $Al2O_3$ may be partially attributed to the rougher surfaces of these substrates in comparison with atomically smooth h-BN substrates. In addition to surface roughness scattering, charged impurities present at the interface between the semiconducting channel and substrate have been widely considered as the primary cause of low room-temperature mobility in TMD devices.[3, 11] Radisavljevic*et al.* recently showed significantly improved mobility in monolayer MoS_2 devices with a high-κ HfO_2 top-gate dielectric, which was attributed to effective damping of Coulomb scattering on charged impurities.[11] The observation of near intrinsic mobility in our MoS_2 devices on h-BN suggests that the h-BN flake not only provide a ultra-smooth and ultraclean channel/substrate interface but also effectively isolate the channel from the influence of the charged impurities in the SiO_2 underneath. On the other hand, although the extremely hydrophobic OTMS on SiO_2 surface is expected to limit water adsorption and suppress charged impurities at the substrate/channel interface, the extremely thin OTMS monolayer may not be thick enough to substantially reduce the long-range Coulomb scattering from the charged impurities in the SiO_2.[61] As a result, the low temperature mobility of our MoS_2 on OTMS modified SiO_2 is similar to that on bare SiO_2. The lower mobility of MoS_2 on Al_2O_3 than on h-BN at low-temperatures suggests that high dielectric constant of Al_2O_3 (ε = 8-9) is inadequate to effectively screen the Coulomb scattering originating from the charged impurities in the Al_2O_3 substrate or at the substrate/channel interfaces. In addition, the rougher surface of Al_2O_3 can further reduce the mobility. Therefore, we can safely

infer that the long-range Coulomb scattering originating from the charged impurities in SiO_2 and Al_2O_3 along with the short-range surface roughness scattering likely limit the low-temperature mobility on SiO_2 (with and without OTMS modification) and Al_2O_3 substrates. Assuming that the mobility on h-BN is not affected by the substrate and surrounding environment, the substrate limited mobility μ_{sub} at 90 K is estimated be approximately 1160 $cm^2V^{-1}s^{-1}$, 990 $cm^2V^{-1}s^{-1}$, and 650 $cm^2V^{-1}s^{-1}$ on SiO_2, OTMS modified SiO_2 and Al_2O_3 respectively, using Mathiessen's rule:

$$\boldsymbol{\mu^{-1} = \mu_{ch}^{-1} + \mu_{sub}^{-1}}$$

where μ_{ch} is the channel contribution and μ_{sub} is the contribution from substrate and environment. At this point our results demonstrate that the scattering mechanisms from non-ideal substrates such as SiO_2 and Al_2O_3 limit the mobility of multilayer MoS_2 to between several hundred and 1000 $cm^2V^{-1}s^{-1}$, which is still at least an order of magnitude higher than the intrinsic phonon limited mobility at room temperature on all substrates. Moreover, the good agreement between the temperature dependence of the mobility from our MoS_2 devices on h-BN and the theory of phonon-limited mobility in MoS_2 further rules out defects and/or native impurities in the MoS_2 as dominant mobility-limiting factors for the temperature range between 77 K and room temperature. The Hall mobility variation with respect to carrier concentration of MoS_2 devices on SiO_2 and h-BN substrates shows complete different behavior at all temperatures. **Fig.3.3.11** (e) and **Fig.3.3.12** (d) depict the Hall mobility variation with carrier concentration at different temperature from room temperature down to 100K on SiO_2 and h-BN substrates respectively. The Hall mobility remains almost same or even decreases with decrease of carrier concentration indicates the charge impurity scattering dominated transport mechanism or competing effect of remote optical phonon scattering and charge impurity scattering originates from SiO_2 substrate. In contrast, the Hall mobility of MoS_2 devices on h-BN increases with

decrease of carrier concentration shows the intrinsic phonon limited transport since the phonon population increase with increase of carrier concentration on channel.

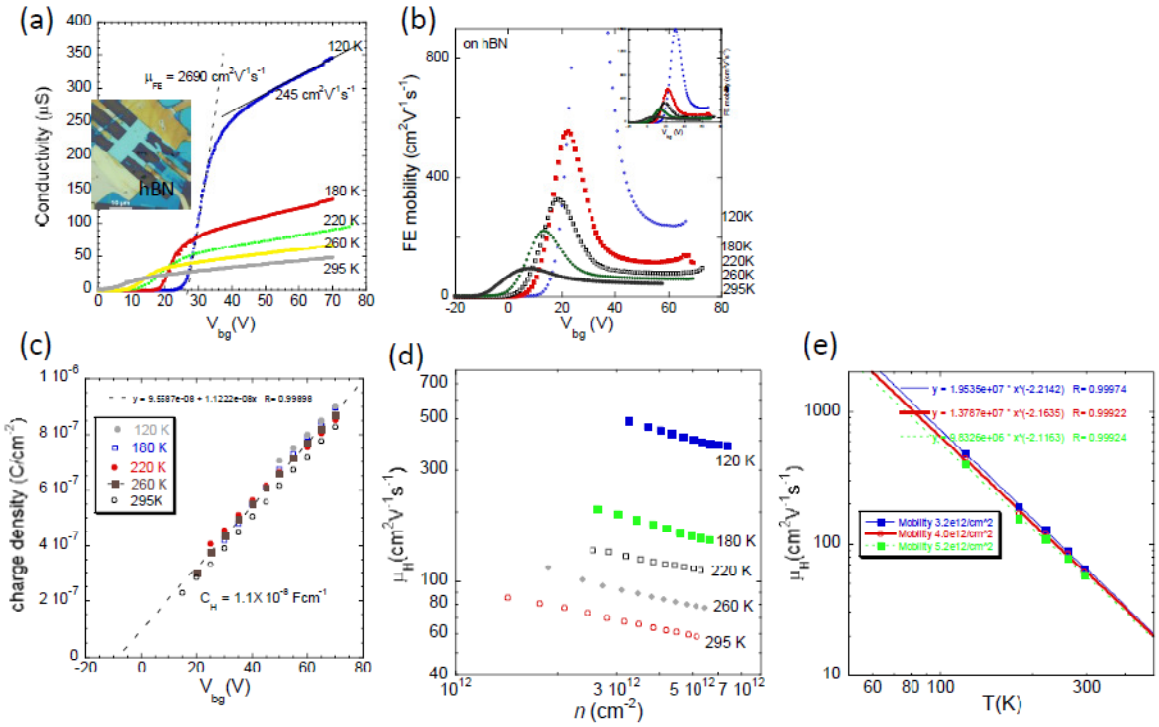

Fig.3.3.12 Gate dependence four (a) probe conductivity (b) four probe field effect mobility (c) charge carrier density at different temperatures on h-BN and hall bar device on h-BN (in inset (a)) (d) carrier concentration dependence hall mobility at different temperatures on h-BN (e) temperature dependence hall mobility at different carrier concentrations on h-BN

3.4 SUMMARY

In summary, we demonstrate reliable fabrication process of MoS_2 field effect transistor devices on different substrate by dry transfer technique. The room-temperature drift mobility in multiplayer MoS_2 at high carrier densities is largely limited by optical-phonon scattering and lies between 40-60 cm^2/Vs. The carrier concentration dependence Hall mobility reveals the intrinsic phonon limited transport mechanism of MoS_2 devices on h-BN substrates while competing effect of coulomb scattering and remote optical phonon scattering mechanism shows on SiO_2 substrate. The mobility of MoS_2 on h-BN substrate is limited by intrinsic phonon scattering down 77 K,

external scattering mechanisms primarily due to substrate-dependent remote phonon scattering and interfacial Coulomb scattering in Al_2O_3 and SiO_2 with or without OTMS surface modification degrades the mobility of MoS_2. The observed stronger temperature dependence mobility (power law exponent γ = 2.2) on ultraclean and atomically smooth h-BN substrate supports intrinsic phonon limited mobility of MoS_2 FET devices.

CHAPTER 4 STUDY THE TEMPERATURE DEPENDENCE TRANSPORT PROPERTIES OF $MoSe_2$ FIELD EFFECT TRANSISTOR ON PARYLENE – C AND SiO_2 SUBSTRATES

4.1 INTRODUCTION

The isolation of graphene by mechanical exfoliation has stimulated research on broad perspective applications of graphene. In addition, graphene has superior properties including mechanical flexibility, extremely high mobility, thermal & chemical stability. But the gapless nature of graphene opened up research on a broad range of other 2D materials family. Layered transition metal dichalcogenides (TMDs) are the members of 2D materials which attracted particular attention after graphene discovered. The semiconducting members of the TMD family including MoS_2, $MoSe_2$, WSe_2, and WS_2 have demonstrated many of the graphene properties highly desirable for electronic applications such as a relatively high mobility, mechanical flexibility, chemical and thermal stability, the absence of dangling bonds and also have a substantial band gap between 1-2 eV which is absent in graphene.[5-19] Due to the substantial band gap TMDs have enough on/off ratio for digital applications. Similar to graphene, atomic layers of covalently bonded chalcogen - metal chalcogen layer can be extracted from bulk TMD crystals by a mechanical cleavage method due to the relatively weak van der Waals interactions between the layers.

Despite this recent progress, the mobility values of monolayer and multilayer TMDs especially MoS_2, $MoSe_2$ and WSe_2 devices on SiO_2 reported by multiple groups were substantially below the Hall mobility of bulk TMDs and substantially below[7, 11, 12, 14, 72-74] than the phonon limited mobility by first principle calculation[58] which greatly hinders their potential applications in multifunctional electronic devices. In addition to the intrinsic scattering from phonons in the TMD channel, the carrier mobility of TMD transistors on SiO_2 is also expected to be limited by

extrinsic scattering like coulomb scattering from charged impurities at the channel/substrate interface & charge traps in SiO_2, substrate surface roughness scattering and remote surface optical phonons scattering originating from substrate. Coulomb scattering from charged impurities& charge traps at the channel/substrate interface has been proposed as the dominant cause of scattering at relatively low room-temperature. Although a high-κ dielectric may screen Coulomb scattering from charged impurities, complete recovery of the intrinsic phonon-limited mobility has not been observed in high-κ dielectric encapsulated TMDs devices. On the other hand, the presence of a low-energy optical phonon mode in SiO_2 (~60 meV) may also cause non-negligible surface polar optical scattering[81] and significantly reduce the mobility especially at high temperatures, as suggested by a recent theoretical study. However, experimental investigations of surface polar optical phonon effects on the channel mobility of TMD FETs are still not fully investigated. In order to device high-performance TMDs channel FETs, it is crucial to use substrate/dielectric materials that do not further reduce the TMD mobility by surface polar optical phonon scattering. Parylene-C is an excellent candidate for substrate because its lowest energy optical phonon mode of 130 meV (corresponding to the vibrational stretch of C-Cl bond) cannot be easily excited at room temperature.[86] Moreover, parylene-C is insoluble in common solvents such as acetone and isopropyl alcohol, thermally stable & chemically inert, low dielectric constant (2.9), hydrophobic oxygen free polymer, conformal uniform coating on SiO_2 and thus comparable with the standard device fabrication process. Parylene-C is a cross-linkable polymer widely used as a passivation layer and gate dielectric in past and recent electronics. A detailed temperature dependent electrical study of ultrahigh crystalline quality TMDs FETs of varying thickness down to single layer on SiO2 and parylene-C substrates able to disentangle the different scattering mechanisms originated from substrate and substrate channel interface.

4.2 EXPERIMENTAL DETAILS

4.2.1 CRYSTAL GROWTH

The $MoSe_2$ crystal is grown by chemical vapor transport method using iodine as a transport agent. Chemical vapor transport (CVT) represents the standard technique to grow high quality crystalline bulk transition metal dichalcogenides. High purity transition metal molybdenum (Mo) and chalcogen selenium (Se) are filled with stoichiometric composition using slight excess selenium into a quartz ampoule together with transport agent iodine (I). The ampoule is introduced into a furnace with a temperature gradient on two sides of it. In the hotter region of the ampoule, the starting materials molybdenum, iodine form MoI_4. The iodide reacts at the molybdenum surface to form MoI_4 is an exothermic reaction and vaporizes completely which reacts with gas form Selenium in the colder side of the ampoule to grow crystalline bulk $MoSe_2$ according to following equation

$$MoI_4 + 2Se \rightarrow MoSe_2 + 2I_2$$

4.2.2 CLEANING THE SUBSTRATE

The degenerately doped silicon substrate with a 290 nm thick thermal oxide layer was used as a substrate to fabricated $MoSe_2$ FET devices or deposits other dielectric to fabricate TMDs FET devices on different dielectric interface. The Si/SiO_2 substrate was sonicated in acetone about 30 minutes and then transferred to isopropanol (IPA). The substrate was again sonicated about 15 minutes in isopropanol and dried by using jet of nitrogen gas. The well dried silicon substrate was put in vacuum and slowly increased its temperature to 600˚C and annealed about 10 minutes by passing Forming gas about 2 minutes. Then the temperature of the vacuum slowly decreased to room temperature. To clean further, the substrate was exposed in oxygen plasma about 5 minutes to remove any impurities on the surface if needed.

4.2.3 PREPARATION OF SAMPLE

4.2.3.1 PREPARATION OF SAMPLE ON Si/SiO_2 SUBSTRATE

Mechanical cleavage method was used to prepare ultra-thin $MoSe_2$ sheets from bulk crystal by using adhesive blue tape. Thin $MoSe_2$ flakes were prepared on scotch tape by repeated splitting of bulk $MoSe_2$ crystal. The thin $MoSe_2$ flakes were transferred on to cleaned degenerately doped silicon substrate having with a 290nm thick silicon dioxide layer. Although we can't control over planer dimensions and thickness of $MoSe_2$ flakes, the flakes are pure and clean as bulk crystals and process of getting thin flakes from bulk crystal is very easier by this method. The better thin flakes were identified by using optical microscope with comparison of color contrast and further relocated by non-contact mode Park System XE - 70 atomic force microscopes (AFM) with respect to prefabricated gold (Au) alignment marks on the silicon substrate. The topographical image of AFM was used to determine thickness, length and breadth of the flakes. **Fig.4.2.1** shows the representative optical image of 8.0 nm $MoSe_2$ sample on Si/SiO_2 substrate and **Fig.4.2.2** represents the AFM image of corresponding flake.

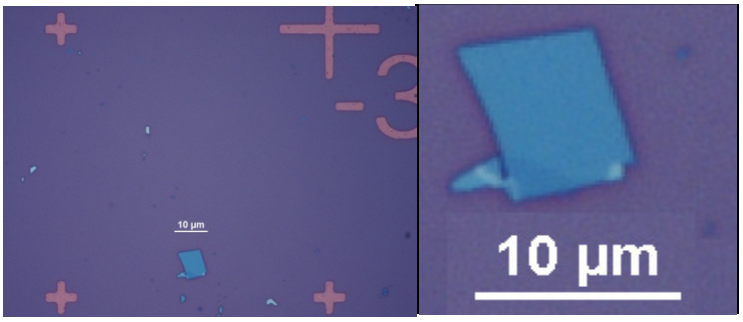

Fig.4.2.1 The left picture indicates the optical microscope image of 8.0 nm $MoSe_2$ sample with gold (Au) alignment marks and the right is close-up image of same sample on Si/SiO_2 substrate.

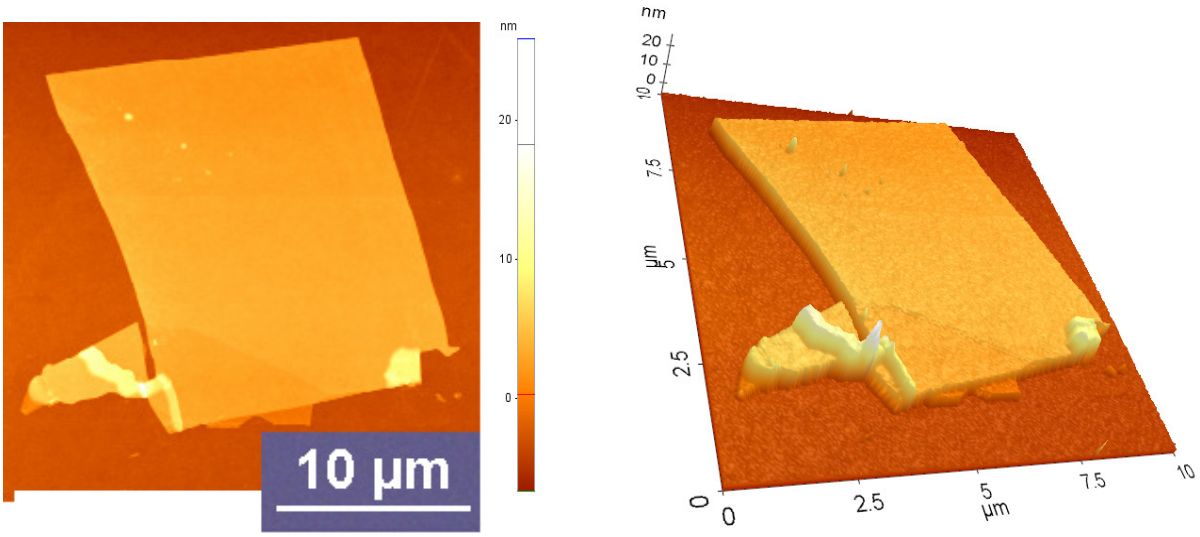

Fig.4.2.2 The left picture is the AFM image of 8.0 nm $MoSe_2$flake and its 3D image on the right on Si/SiO_2 substrate.

4.2.3.2 PREPARATION OF SAMPLE ON PARYLENE – C SUBSTRATE

A pre-cleaned highly p-doped silicon substrate with 290 nm of thermally grown SiO_2 by acetone and isoproponal (IPA) was treated by oxygen plasma for 10 min to clean the surface of the substrate thoroughly. Parylene-C was deposited on Si/SiO_2 at room temperature using di-paraxylyene (DPX) as the precursor in a commercially available parylene coating system (PDS 2010). Multilayer $MoSe_2$ flakes were produced by mechanical exfoliation of high-quality $MoSe_2$ crystals and subsequently transferred to Si/SiO_2 substrates with and without 130 nm of parylene-C. Optical microscopy and Park-Systems XE-70 non-contact mode atomic microscopy were used to identify and characterize ultrathin $MoSe_2$ flakes.

4.2.4 FABRICATION OF $MoSe_2$ FET DEVICES

In order to measure the electric properties, it is necessary to fabricate the electrodes for electrical connections. Nanometer Pattern Generation System (NPGS) software was used to draw the electrodes pattern and conventional electron beam lithography was used to define electrodes. Two layers of electron resist polymer Polymethyl methacrylate (PMMA), 495-A4 and 950-A2

(same polymer having different molecular weight), were spin coated followed by 180˚C baking on the hotplate for 5 min after coating of each layer. Scanning electron microscope (Hitachi S-2400) was used to define electrodes pattern. The optimization of SEM by adjusting beam current, fine focus with minimizing astigmatism of focus electron beam and adjustment of different parameters like beam current, writing dose (area or line), alignment of alignment marks of substrate is critical for electron beam lithography. Normally, the current kept around 10 pA to write narrower electrodes and the doses were set to be 10nC/cm for line and 260 $\mu C/cm^2$ for area. The substrate was soaked in isobutylketone (MIBK) for 70 seconds to develop the e-beam writing electrodes. A chemical MEK was used to enhance the developing process.

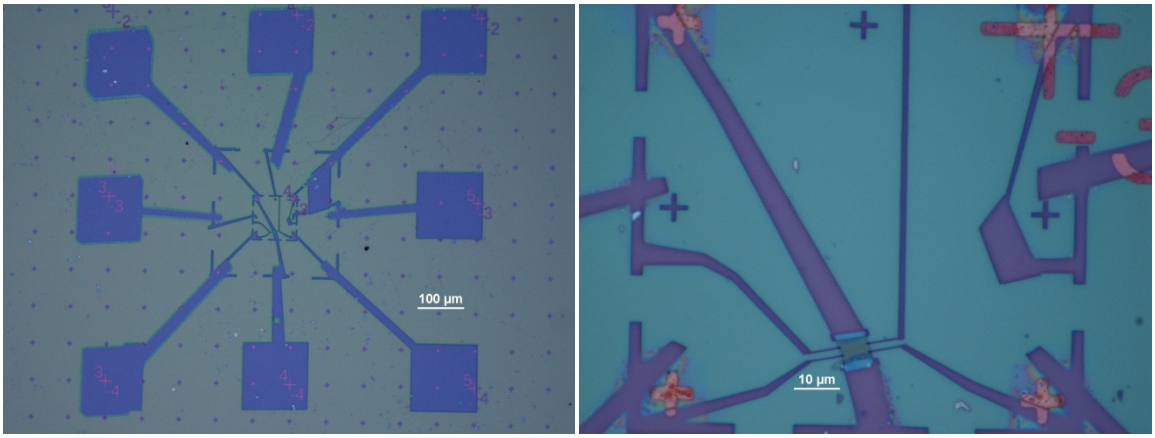

Fig.4.2.3 The left image is defined electrodes after completing electron beam lithography process under optical microscope with magnification 10x. The right image is close-up image of narrower electrodes under optical microscope with magnification 100x.

For deposition of metal on electrodes, BJD-1800 e-beam metal evaporator was used. The substrate with electrode pattern after e-beam lithography was fixed on the hood of the metal evaporator. 5nm titanium (Ti) and 50 nm gold (Au) were deposited at ultrahigh vacuum (about 10^{-7}torr) with deposition rate 1˚A/s.

Fig.4.2.4 The schematic diagrams show the integrated processes with electron beam lithography and metal deposition, BJD 1800 e-beam metal evaporator and the device after gold deposition.

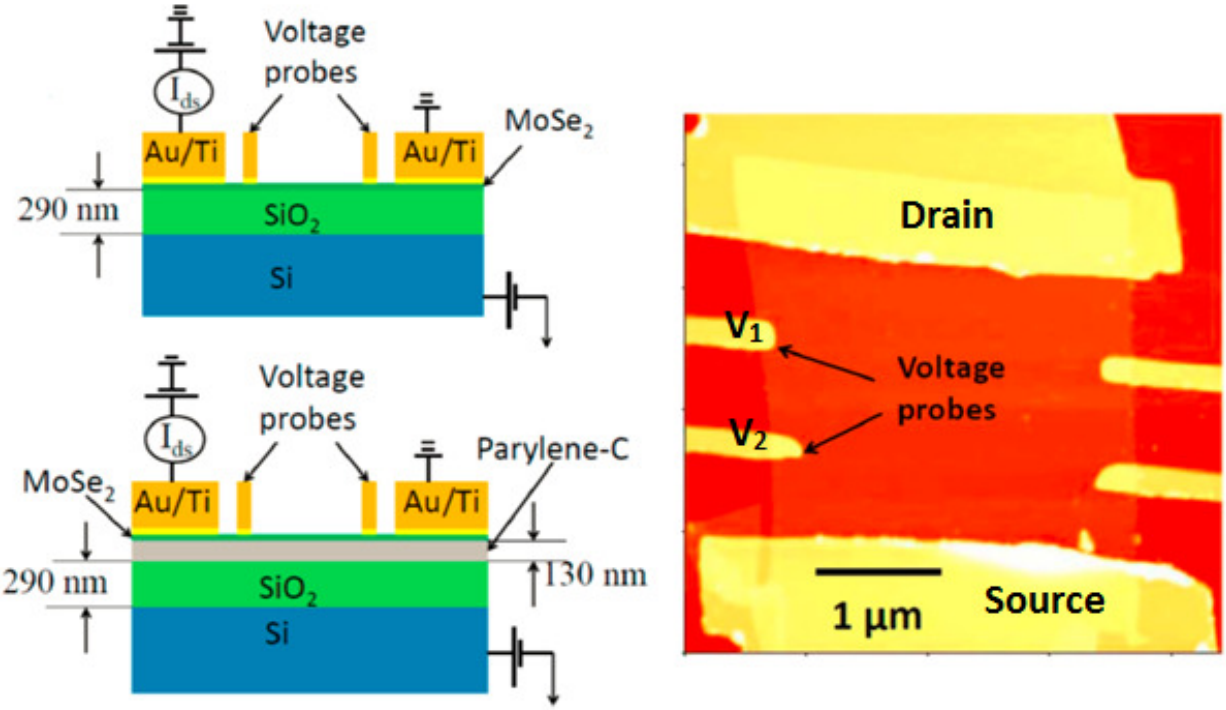

Fig.4.2.5 The schematic diagrams show the schematic diagram of device on Si/SiO_2 and Si/SiO_2/Parylene-C substrates and the 8.0 nm $MoSe_2$device after gold deposition

Acetone was used for lift off to get designed device electrodes. The device was kept in cryogenic probe station (Lakeshore Cryogenic probe station) under ultrahigh vacuum (~10^{-6} to 10^{-7} torr) and measured its electrical transport properties by a Keithley 4200 semiconductor parameter analyzer at various temperature (77 K <*T* < 300 K). Liquid nitrogen and temperature controlled heater were used for temperature dependence (77K -300K) electrical transport

measurements. **Fig.4.2.5** The schematic diagrams show the schematic diagram of $MoSe_2$ device on Si/SiO_2 and Si/SiO_2/Parylene-C substrates and the $MoSe_2$ device after gold deposition.

4.3RESULTS AND SISCUSSION

4.3.1 STM/STS STUDY OF $MoSe_2$ CRYSTAL AND BAND GAP ESTIMATION

STM/STS measurements were performed on freshly cleaved surfaces of $MoSe_2$ crystals inside ultra-high vacuum (UHV) chamber at 4.5 K without any additional thermal treatment (to avoid any possible thermally induced surface reconstruction). **Fig.4.3.1 (a)** shows a representative STM topographic image of cleaved $MoSe_2$ surface, where the atomically resolved honeycomb and spherical structures bare close resemblance to other layered systems such as MoS_2 and graphene. The 1×1 unit cell is shown as a rhombus in the high resolution image (**Fig.4.3.1 (b)**) with a lattice distance of 3.4 Å similar to previously reported value. According to previous report, Se localized orbital can be resolved and Se sublattice is shown in STM image.[87] The 2 nm by 2 nm relatively large surface scan area shows clean and nearly defect/impurity free surface.

We performed **STS** spectroscopy (d*I*/*dV* vs. bias voltage) using a lock-in technique. As shown in Fig. b, the STS spectra exhibit a gap with a width of ~ 1.45 eV. However, three distinctive peaks appear in the gap region, may correspond to the indirect band-gap of a monolayer $MoSe_2$.[88-91] More interestingly, three distinctive peaks can be observed inside the gap in all the spectra measured at randomly selected locations on the nearly defect-free surface, suggesting an intrinsic electronic structure of $MoSe_2$ rather than impurity states. Furthermore, their energy levels can be well associated with the three minima in the conduction band of bulk $MoSe_2$, in quantitative agreement with the results from density functional theory (DFT) band-structure calculations. [88] According to the density functional theory (DFT) calculations, the band

structure of bulk $MoSe_2$ displays indirect band-gaps of 0.84 eV, 1.10 eV and a 1.34 eV direct band-gap. In contrast, for single-layer $MoSe_2$, it becomes a direct band-gap semiconductor with a 1.34 eV gap value at the K symmetry point. Such direct band-gap transition at the two degenerate valleys is induced by inversion symmetry broken of single layer $MoSe_2$. Since STM is surface-sensitive technique and surface is the top layer of bulk with inversion symmetry broken, thus the direct band-gap at the K point will be more dominant than other indirect band-gaps. The gap measured from STS spectra about 1.45 eV, suggests strongly it is the direct band-gap of $MoSe_2$ on the surface.

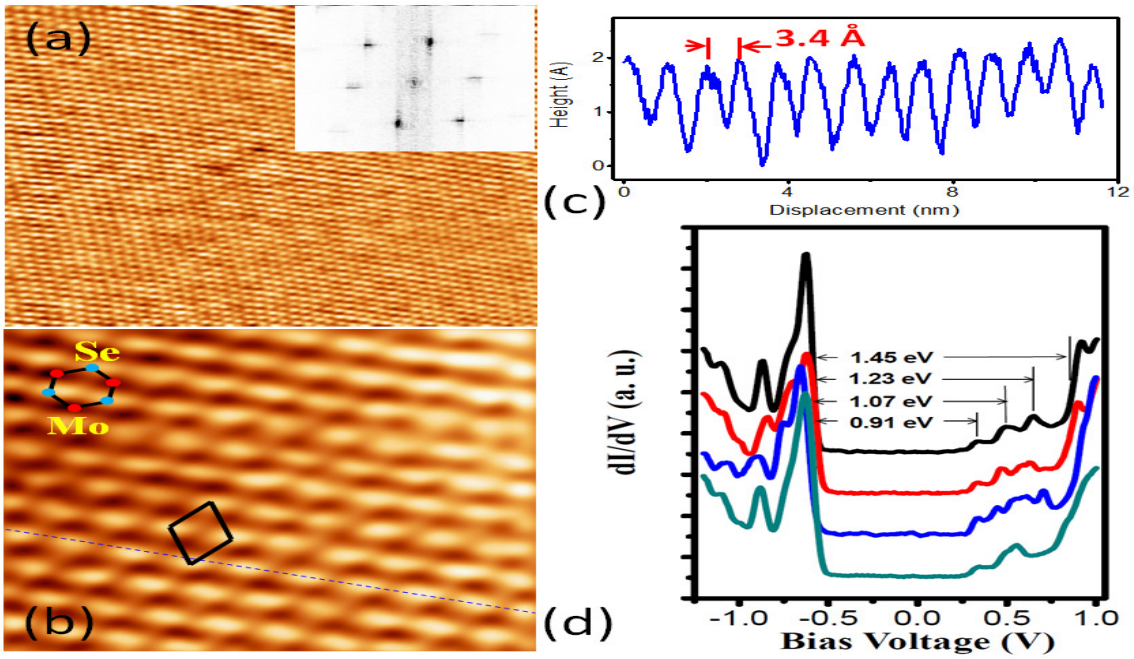

Fig.4.3.1 (a) Atomic resolution STM topography (V_{bias}= -0.5 V, I_{set}= 100 pA) of a cleaved $MoSe_2$ crystal measured at 4.5 K. (b) Close-up image showing a defect-free hexagonal lattice. (c) Line profile showing atomic distance of hexagonal lattice, measured about 3.4 Å, indicates STM visualizing one of the sublattices of $MoSe_2$. (d) STS spectra measured at randomly selected locations on the surface of the same crystal, exhibit a gap with the size of 1.45 eV and in-gap DOS. All spectra were taken with a sample-bias voltage of 100 mV, a tunneling current of 0.1 nA, and bias modulation amplitude of 5 mV_{rms}.

4.3.2 ELECTRICAL TRANSPORT PROPERTIES AT ROOM TEMPERATURE

$MoSe_2$ FET devices were fabricated using standard electron beam lithography and electron beam deposition of 5 nm of Ti and 50 nm of Au. To eliminate electrical contact contributions, we also patterned voltage probes in between drain and source electrodes to facilitate four-terminal measurements. Electrical properties of the devices were measured by a Keithley 4200 semiconductor parameter analyzer in a Lakeshore Cryogenic probe station under high vacuum (~ 1×10^{-6} torr). First of all, we characterized the drain source I-V characteristics at room temperature to test the quality of Ti/Au contacts on $MoSe_2$.**Fig.4.3.2** (c) and (d) depicts representative drain source current voltage curve of $MoSe_2$ devices at different back gate voltage on SiO_2 and parylene-C, respectively. It shows the drain-source current of both devices is linear at high back gate voltages. As V_{ds} increases, the drain-source current starts to saturate in the low gate voltage range (V_{bg}< 10 V and < 30 V for both devices), while remaining linear at higher gate voltages. The current saturation at low gate voltages is likely caused by the reduction of the effective V_{bg} and V_{ds} due to the relatively large parasitic series drain/source contact resistance (R_C) given by $V_{bg\_eff}= V_{bg} - R_C I_{ds}$ and $V_{ds\_eff} = V_{ds} - 2R_C I_{ds}$.[19] At higher V_{bg}, the contact resistance is lowered by the reduction of the effective Schottky barrier height through band bending, which leads to more linear I_{ds}-V_{ds} behavior signifying near ohmic contacts.[77] This test suggests that it is able to get the channel properties at sufficiently large back gate voltage. We measured its room temperature transfer characteristics of both $MoSe_2$ devices. Both devices show asymmetric ambipolar behavior. The on current of electrons carrier is much higher than holes carrier with ON/OFF current ratio exceeding 10^6 for electrons and less than 10^3 for holes at V_{ds} = 1 V. The asymmetry between electron and hole transport primarily due to relatively large Schottky barrier for the holes as the Fermi level of the contact metal titanium tends to line up much closer to the conduction band edge in $MoSe_2$and the effect add up by small amount of intrinsic *n*-doping in

the $MoSe_2$ channel.[92] The observed hysteresis is likely due to the charge injection from the adsorbates (such as moisture and oxygen) and/or charge traps on the channel surfaces and/or at the interfaces between the channel and the substrate.[93] To investigate the electronic properties of $MoSe_2$ channel at room temperature, we extracted the back gate voltage dependence conductivity of $MoSe_2$ FETs from its transfer characteristics measurements on SiO_2 and parylene-C. **Fig. 4.3.3 (a)** shows the room temperature back gate dependence conductivity for two representative $MoSe_2$ devices on SiO_2 and parylene-C. Conductivity is defined as:

$\boldsymbol{\sigma = \frac{L}{W} \times I_{ds} \times / V_{in}}$, where L and W are the distance between inner voltage probes and sample width respectively and V_{in} is the measured voltage difference between the inner voltage probes by applying low bias voltage V_{ds} = 50 mV in all measurements. In spite of the qualitatively similar transfer and output characteristics $MoSe_2$ devices on SiO_2 and parylene-C (**Fig.4.3.2**), the conductivity of the $MoSe_2$ device on parylene-C is significantly steeper than that on SiO_2. To eliminate any possible sample variations, we systematically measured 11 $MoSe_2$ devices on SiO_2 and 5 $MoSe_2$ devices on parylene-C in the four-terminal configuration. The global field-effect mobility is extracted from the gate dependence conductivity curve using the expression $\mu = d\sigma/dV_{bg} \times 1/C_{bg}$ in the high back gate voltage linear region, where C_{bg} is the back-gate capacitance per unit area. Based on parallel plate capacitor model, C_{bg} is determined to be 1.2 $\times 10^{-8}$ F cm^{-2} for 290 nm SiO_2 ($C_{bg} = \kappa \times \varepsilon_0/d$ nm, κ =3.9 for SiO_2) and 7.6 $\times 10^{-9}$ F cm^{-2} for 130 nm parylene-C on 290 nm SiO_2 by series combination of them ($\boldsymbol{C_{bg} = \frac{3.9 \times 3.12 \times \varepsilon 0}{130\ nm \times 3.9 + 290\ nm \times 3.12}}$, κ =3.12 and 3.9 for parylene-C and SiO_2 respectively).[83] **Fig. 4.3.3 (b)** is thickness dependence room temperature field-effect for all $MoSe_2$ devices, with thickness ranging from ~ 5 nm to 14 nm. The mobility of $MoSe_2$ devices on SiO_2 fluctuates around an average value of ~50 $cm^2V^{-1}s^{-1}$ without showing any noticeable thickness dependence,

consistent with previous results from SiO_2-supported multilayer MoS_2.[94] In spite of the extremely high crystalline quality of our $MoSe_2$ samples (**Fig. 4.3.1 (a)**), the room temperature mobility of $MoSe_2$ devices on SiO_2 substrate is rather low compared to the Hall mobility of bulk $MoSe_2$ (100 $cm^2V^{-1}s^{-1}$ – 200 $cm^2V^{-1}s^{-1}$), but it is similar to that observed MoS_2 devices on SiO_2 fabricated from commercially available MoS_2crystals.[47, 84] In contrast, the room temperature mobility of $MoSe_2$ devices on parylene-C ranges from ≈100 $cm^2V^{-1}V^{-1}s^{-1}$ to ≈150 $cm^2V^{-1}V^{-1}s^{-1}$, which is close to the bulk values.[84] This suggests that the room temperature mobility of our $MoSe_2$ devices on SiO_2 is likely limited by extrinsic scattering mechanisms. To investigate details mechanism, we measured variable temperature measurements.

4.3.3 ELECTRICAL TRANSPORT PROPERTIES AT LOW TEMPERATURES AND DIFFERENT SCATTERING MECHANISMS

To identify the quality of Ti/Au contacts on $MoSe_2$, we characterized the I-V characteristics at 77K. **Fig. 4.3.4** represents drain source current voltage curve $MoSe_2$ devices on SiO_2 and parylene-C as title in figures. The current shows non-linear relation with drain source voltage at low back gate voltage (as shown **Fig. 4.3.4 b**) indicating significant schottky barrier at low back gate voltage and the current becomes linear at sufficiently large back voltage (as shown **Fig. 4.3.4** a, c) suggesting the contact resistance is significantly lower than the channel resistance at high back gate voltage. To understand the transport mechanism and role of dielectric of $MoSe_2$ channel, we measured back gate transfer characteristics of $MoSe_2$ FETs on SiO_2 and parylene-C substrates at different temperatures form room temperature down to 77K and extracted the back gate dependence conductivity.

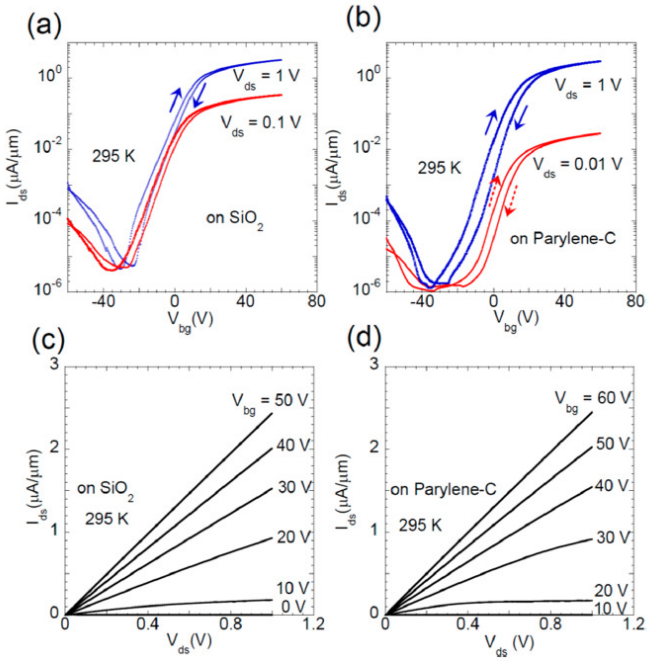

Fig. 4.3.2 Room temperature transfer curve of $MoSe_2$ FET fabricated (a) on SiO_2 and (b) on parylene-C. Room temperature output curve of $MoSe_2$ FET fabricated (c) on SiO_2 and (d) on parylene-C of the same devices (a) and (b) respectively.

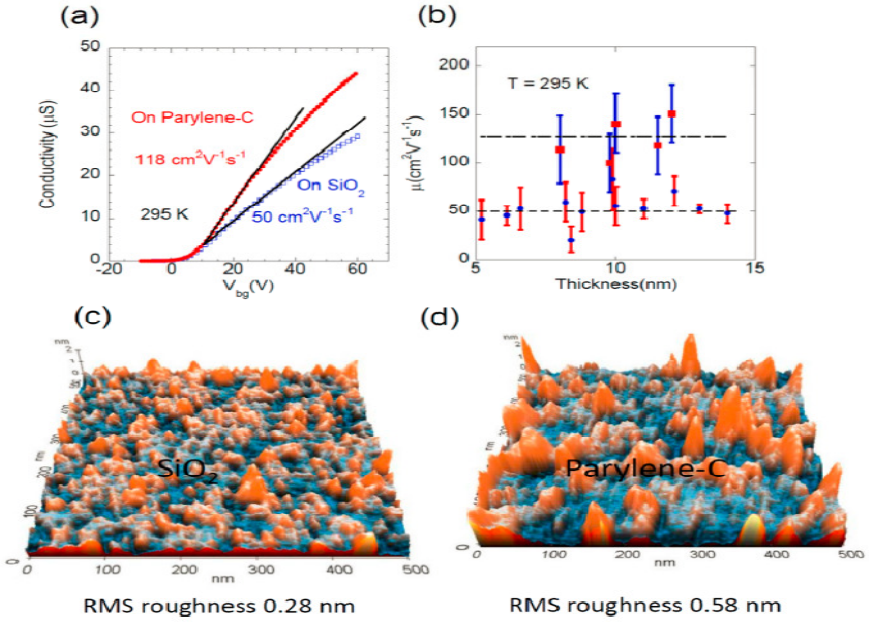

Fig.4.3.3 (a) Room temperature 4-terminal conductivity of $MoSe_2$ FET fabricated on SiO_2 and on parylene-C. (b) Field effect mobility as a function of $MoSe_2$ thickness from multiple $MoSe_2$ FET devices fabricated on SiO_2 indicated by blue circle and parylene-C indicated by redsquare.(c,d) AFM image of SiO2 and parylene-C surfaces respectively.

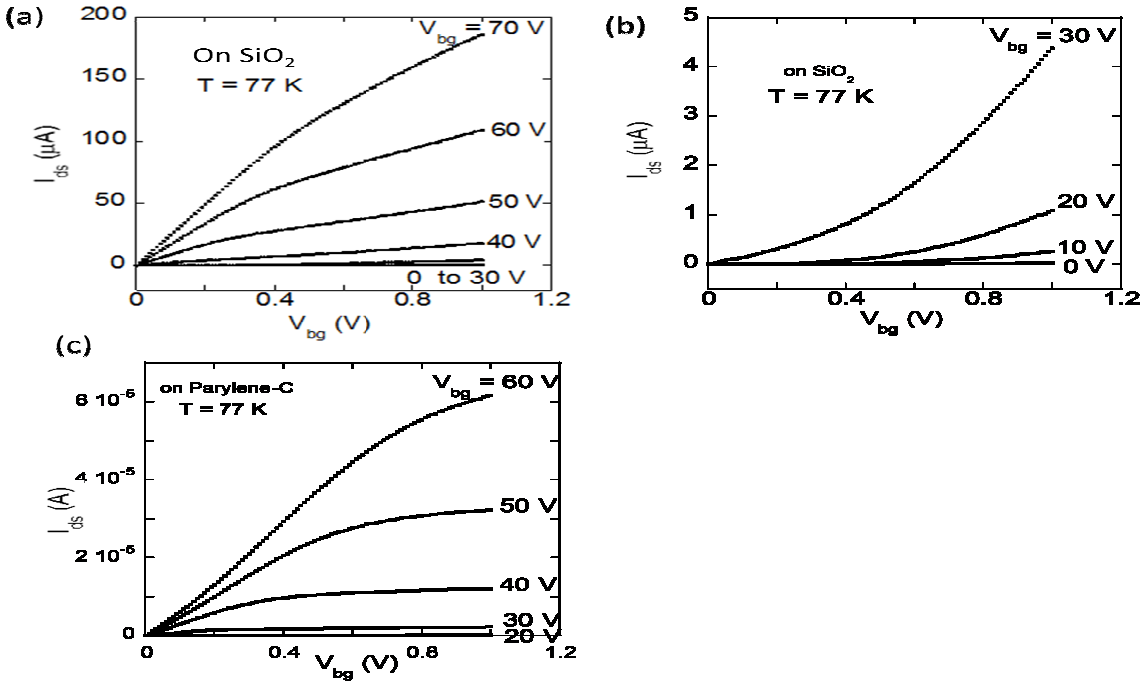

Fig. 4.3.4 output curve of $MoSe_2$ FET fabricated on SiO_2at 77K (a) at high V_{bg} and (b) at low V_{bg} (c) output curve of $MoSe_2$ FET fabricated on parylene-C

To understand the extrinsic and intrinsic effects on the mobiltiy in our $MoSe_2$ devices, we consider various mobility-limiting scattering mechanisms according to Mathiessen's rule:

$$\boldsymbol{\mu^{-1} = \mu_{INT}^{-1} + \mu_{SD}^{-1} + \mu_{CI}^{-1} + \mu_{SR}^{-1} + \mu_{SPP}^{-1}}$$

Here μ_{INT}^{-1} represents the mobility limited by intrinsic lattice phonons scattering, μ_{SD}^{-1} is mobility limited by structural defects, and μ_{CI}^{-1}, μ_{SR}^{-1} and μ_{SPP}^{-1} represent mobility limited by Coulomb impurities (CI) and charge traps, the surface roughness (SR), and the dielectric surface polar optical phonons (SPP), respectively. The intrinsic mobility $\mu_{INT}$and mobility limited by structural defects μ_{SD} are expected to be similar for $MoSe_2$ FETs both on SiO_2 and on parylene-C, since all our devices are fabricated from the same $MoSe_2$ crystal. We also exclude structural defects as a major source of scattering given the extremely high crystalline quality of our $MoSe_2$ crystals verified by STM measurements. Next, we consider the effects of surface roughness

scattering on the mobility of our $MoSe_2$ devices. **Fig.4.3.3** (c) and (d) show AFM topographic images on SiO_2 and parylene-C in the vicinity of $MoSe_2$ samples, respectively. We observed RMS surface roughness is 0.3 nm for SiO_2 and 0.6 nm for parylene-C. The observation of higher mobility on rougher parylene-C substrate rules out surface roughness scattering as a major cause of the substrate dependent mobility in our $MoSe_2$ devices. Therefore, we can safely deduce that the lower mobility in $MoSe_2$ devices on SiO_2 is likely due to additional Coulomb scattering and/or surface polar optical phonon scattering introduced by substrate.

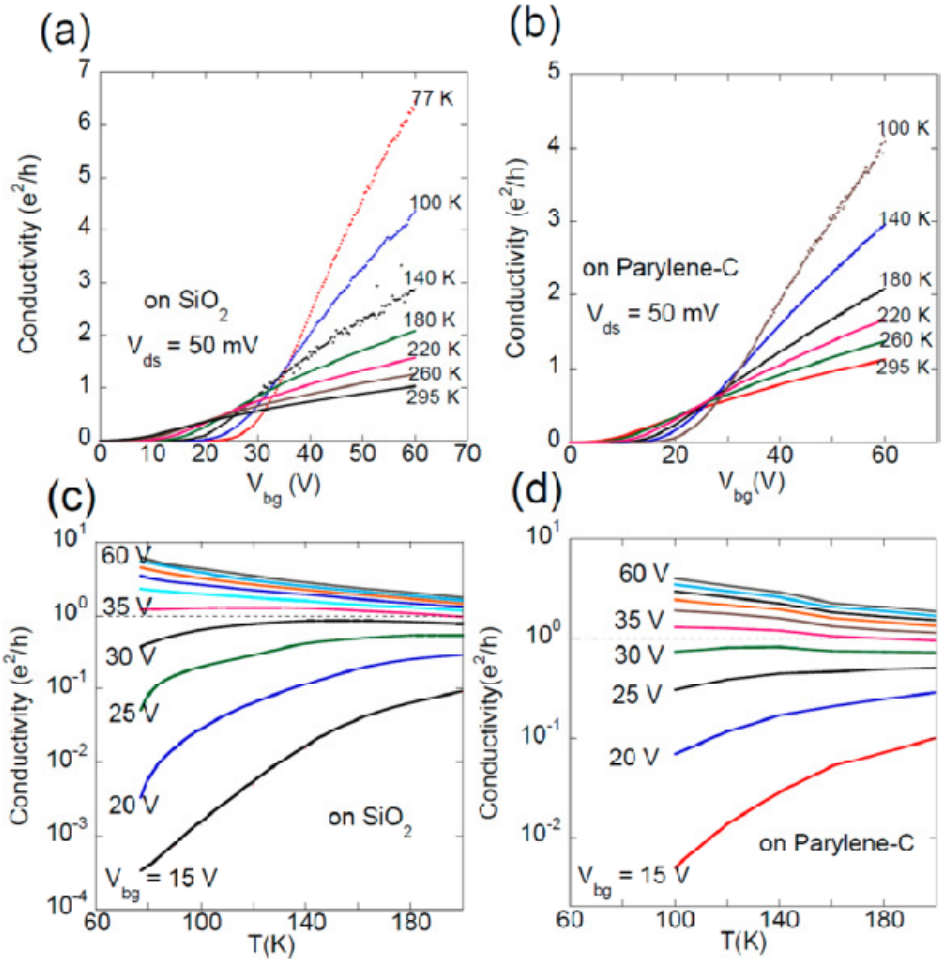

Fig. 4.3.5 (a,b) Temperature dependence 4-terminal conductivity of $MoSe_2$ FET fabricated on SiO_2 and on parylene-C respectively. (c,d) Gate voltage dependence 4-terminal conductivity as a function of temperature for the same device in (a) and (b) respectively.

Charged impurities present at the interface between the semiconducting channel and substrate have been generally considered as the primary cause of low room-temperature mobility in TMDs devices.[3, 11] Recent study of monolayer MoS_2 devices with a high-κ HfO_2 top-gate dielectric showed improvement mobility by effectively damping the Coulomb scattering on charged impurities.[11] However, the mobility observed in their MoS_2 devices (up to 60 $cm^2V^{-1}s^{-1}$ at 260K) is still much lower than the theoretical values or experimental results from bulk samples.[58, 84] A possible cause of this discrepancy is surface polar optical phonon scattering from substrate and gate dielectric. Considerable mobility improvement was also reported in multiplayer MoS_2 on PMMA dielectric, which was attributed to the reduced short-range disorder and long range disorder at the channel/PMMA interface than at the channel/SiO_2 interface.[47] However, the lack of low temperature measurement makes it difficult to further ellucidate the origin of substrate dependent mobility in these devices.

Sample name	sample location	Sample thickness	Sample dimensions	4-p RT mobility $cm^2/V.s$	4-p Low T mobility $cm^2/V.s$	2-p RT mobility $cm^2/V.s$	2-p Low-T mobility $cm^2/V.s$
08-12-13-$MoSe_2$ No2 on 290 nm SiO_2	4-1_45	11nm	W= 5.7µm L_{inner}=2.6 µm (2.4~2.8 um) L_{outer}=6.6 µm	52	92 (200K) 144 (100K)		
	1-2_15 left	12nm	W= 5.5µm L_{inner}=4.6 µm (4.4~5.8 um) L_{outer}=12.5 µm	62	138 (200K) 408(100K)		
	1-2_15 right	14nm	W= 4.1µm L_{inner}=5.2 µm L_{outer}=14.5 µm	48	128 (200K) 206 (120K)		
	-64_25	12.5nm	W=3.2µm L(Inner)=1.75 (1.5-1.9) µm L_{outer}=4.7 µm	54			

06-26-23-$MoSe_2$ No3 on 290 nm SiO_2	-5-2_53	8-8.5nm	W=6.4 μm L_{inner}=2.8(2.3-3.3) μm				
06-26-23-$MoSe_2$ No4 on 290 nm SiO_2	-5-5_32	10nm	W= 4.9μm L_{inner}=2.3 μm L_{outer}=6.2 μm	56	104(200K) 256(100K)		
03-26-13-$MoSe_2$ No2 on 290 nm SiO_2	06_44	6.1 nm	W= 2.1μm L_{inner}=2.2 μm (2~2.5 um) L_{outer}=6.0μm	45 (41-51)	83 (200K) 99(180K)	77	
	14_52	5.2 nm	W= 5.4 μm L_{inner}=2.4 μm (1.8~2.9 μm) L_{outer}=6.5 μm	43 (32~ 52)	94 (200K) 106(180K)	65	
03-26-13-$MoSe_2$ No3 on 290 nm SiO_2	-54_45	9.9 nm	W= 4.3 μm L_{inner}=1.5μm (1.3~1.9 μm) L_{outer}= 4.0 μm	78 (67~99)			
03-26-13-$MoSe_2$ No4 on 290 nm SiO_2	-0-0_33	6.6 nm	W= 2.6 μm L_{inner}= 2.5μm (2.0~3.1 μm) L_{outer}= 8.0 μm	52 (42~64)	111(200K) 131(180K) 165(140K) 175(100K)	72	
	3-3_15	6.8 nm	W= 6.1 μm L_{inner}= 1.7μm (1.5~2.1 μm) L_{outer}= 4.6 μm	57 (50~70)	84(200K)	69	
02-18-13-$MoSe_2$ No1 on 290 nm SiO_2	02_45	8 nm	W= 1.8 μm L_{inner}= 2μm (1.3~2.5 μm) L_{outer}= 4.5 μm	52 (34~65)		40	
02-18-12-$MoSe_2$ No3 on 290 nm SiO_2	-06_53	8nm	W=1.7 μm L_{inner}=1.9 μm (1.4~2.5 μm) L_{outer}= 4.4μm	21 (15~28)	34(200K)	28	
12-10-12-$MoSe_2$-No1 on	-31_21	14nm	W=3.2um L=3.2um			50	88(200K) 133(100K)

290 nm SiO_2							
	0-0_23	3.5nm	W=1.7um L=2um			9.5	
	2-5_54	8-11nm	W=2.2um L=1.7um			7.6	
	-2-2_44	5.8nm	W=2.0 µm L=1.4 µm			50	98(200K)
	4-3_52 Bottom electrodes	11nm					
07-15-13 No 1 on 130 nm parylene-C	-06_21	11.7nm	L/W=11.2/3.6 L_{inner}=4.4(3.6-5) µm	118			
	-50_52	10nm	L/W=4.2/4 L_{inner}=2(1-2.9) µm	141			
	-03_43	8nm	L/W=9.6/6.2 L_{inner}=3.3(2.33-4.2) µm	114			
07-15-13 No 2 on 130 nm parylene-C	2-0_13	9.8nm	L/W=2.9/3 L_{inner}=1.1(0.64-1.6) µm	100			
	04_33	12nm	L/W=10.2/16.5 L_{inner}=3.6(2.6-4.2) µm	150			

Table 4.3.1 Different thickness $MoSe_2$ FET devices mobilities fabricated on (a) 290 nm SiO_2 (b) 130 nm Parylene-C on the top of 290 nm SiO_2

To further explore the origin of the mobility difference between $MoSe_2$ devices on SiO_2 and on parylene-C, we systematically extracted the temperature dependence conductivity from four terminal measurements. **Fig. 4.3.5** (a) and (b) show the temperature dependence of conductivity *vs* back gate voltage for two representative $MoSe_2$ devices on SiO_2 and parylene-C. Clearly there are two regions for devices on SiO_2 and parylene-C substrates, insulating or semiconducting section at low back gate with conductivity increases with temperature and

metallic section at high back gate with conductivity decreases with increase of temperature. The cross over from metallic to insulating region is at a critical conductivity of e^2/h, consistent with metal-insulator transition (MIT) observed in monolayer, bilayer and multiplayer MoS_2 as well as theoretical expectations for 2D semiconductors.[11,12, 15] We calculated the critical back gate voltage between 30 and 35 V which corresponding to a critical carrier density of ~ 1×10^{12} cm^{-2} and ~ 7×10^{11} cm^{-2} for the SiO_2 and parylene-C substrates, respectively as shown in **Fig. 4.3.5** (c) and (d).

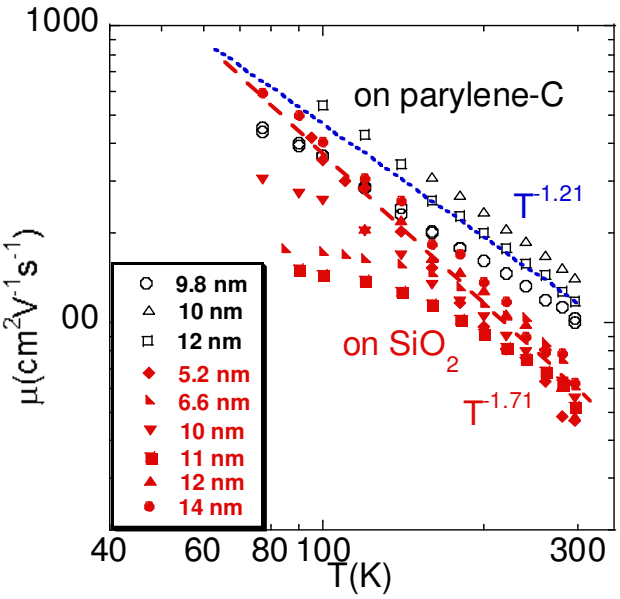

Fig. 4.3.6 Temperature dependence field effect mobility of $MoSe_2$ FET devices on SiO_2 with red solid symbols and parylyne-C with hollow black symbol

Then We calculated the temperature depedence fileld effect moblity from the temperature deppendence conductivity curve on both substrates from the linear region of the conductivity curves in the metallic state (35 <V_{bg}<55V), using the expression for field-effect mobility$\mu = 1/C_{bg} \times d\sigma/dV_{bg}$.**Fig. 4.3.6**shows temperature dependence field effect mobility of $MoSe_2$ FET devices on SiO_2 (solid red symbols) and parylyne-C (hollow blue symbols) with different thicknesses between 5 nm to 14 nm. We fitted the power law of temperature dependence

mobility as a $\mu \sim T^{-\gamma}$. The mobility values of all devices on parylene-C follow $\gamma \approx 1.2$ for the entire measured temperature range. This is consistent with the theoretical modeling of phonon-limited mobility in layered TMD materials such as MoS_2 and $MoSe_2$, which shows $\mu \sim T^{-\gamma}$ dependence where the exponent γ depends on the dominant phonon scattering mechanism with γ~2.4 in bulk $MoSe_2$ samples and lower for carriers in 2D.[58, 84] The relatively low γ in our devices suggests that the charge carriers are likely confined in 2D and behave as a 2D electron gas, which is consist with the recent finding of Li *et al.* that the carriers in a 14 layer MoS_2 FET (about 10 nm thick) are largely confined within 1-2 nm range near the interface of the gated dielectric.[82] On the other hand, the mobility values of all devices on SiO_2 follow a higher $\gamma \approx 1.7$, indicating that their mobility is also predominantly limited by phonon scattering. The mobility of other four $MoSe_2$ device on SiO_2 also follows the same phonon limited behavior (with the same power exponent $\gamma \approx 1.7$) at temperatures above 160 K. As the temperature decreases from 160 K to 77 K, their mobility starts to saturate, likely limited by Coulomb scattering due to the varying amount of charged impurities at the $MoSe_2/SiO_2$ interface as previously observed in MoS_2 devices.[11, 14] Higher γ value for $MoSe_2$ devices on SiO_2 than on parylene-C suggests additional temperature dependent scattering mechanism(s) in SiO_2-supported $MoSe_2$ devices.

The SiO_2 surface has low polar optical phonon mode ($\approx$ 60 meV) can be excited by thermal energy at room temperature, while parylene-C has much higher surface polar optical phonon mode ($\approx$ 130 meV). [95, 96] At about and below 100 K, mobility values for $MoSe_2$ devices on both SiO_2 and parylene-C (those with lower level of charged impurities) merge, which is expected as the mobility being dominated by optical phonon scattering (including surface polar optical phonons).[58] And the observed saturation of mobility at low temperature for some devices is primarily cause by coulomb scattering which is dominated scattering over phonon scattering at

low temperature. The stronger temperature dependence of the mobility $MoSe_2$ devices on SiO_2 might be enhanced charge impurities/traps at the $SiO_2/MoSe_2$ interface than at the parylene-C/$MoSe_2$ interface. Recently, Ong and Fischetti showed theoretically that the increase of mobility with decreasing temperature, which is commonly interpreted to be a signature of phonon-limited electron transport, could also be limited by CI scattering due to the weakening of charge screening within the TMD channel as the temperature increases.[97] However, we believe that the lower room temperature mobility and larger γ in our $MoSe_2$ devices on SiO_2 than on parylene-C substrate is unlikely to be chiefly caused by stronger CI scattering for the following reasons. Firstly, the mobility of all six $MoSe_2$ devices on SiO_2 converges above 200 K in spite of the notable variation of charged impurities as indicated by the strongly sample dependent low temperature mobility, indicating that the high temperature (> 200 K) mobility in these devices is nearly independent of the charged impurities. Secondly, the mobility values of our devices on both SiO_2 and parylene-C are significantly higher than the CI limited mobility from the calculations of Ong and Fischetti, suggesting that CI scattering plays a less significant role in our devices compared to the theory.[97] Thirdly, the temperature dependence of mobility in our devices is qualitatively different from the previously reported CI scattering limited field-effect mobility of MoS_2 devices, in which case the mobility decreases with decreasing temperature below 200 K.[11]

High-κ dielectric like HfO_2 has been favored as a dielectric material for TMD transistors due to its capability to screen charged impurities and its effectiveness in tuning the charge carriers.[9, 11] However, the presence of a soft polar phonon vibration mode in HfO_2 along with its high dielectric constant may lead to severe surface polar optical phonon scattering. [98] A thin layer of parylene-C may serve as a buffer layer between the TMDs channel and high-κ dielectric

like HfO_2, TiO_2, Ta_2O_5 to reduce the surface polar phonon scattering while taking advantage of its high dielectric constant to effectively screen the charged impurities and tune the charge density in the TMDs channel.

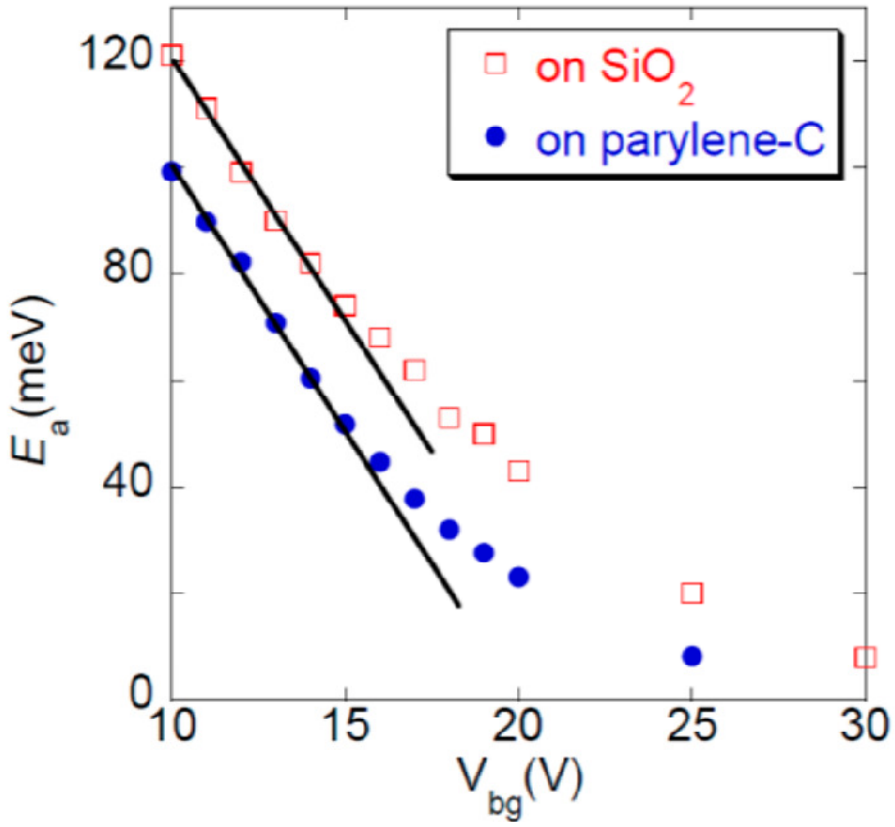

Fig. 4.3.7 Back gate dependence of activation energy of $MoSe_2$ devices on parylene-C and SiO_2 substrates

4.3.4 ACTIVATION ENERGY AND SCHOTTKY BARRIER

Activation energy, E_a, can be extracted using the thermal activation model,

$$\sigma \alpha e^{(-\frac{E_a}{k_B T})}$$

where k_B is the Boltzmann constant and T is absolute temperature. As shown in **Fig. 4.3.7**, the activation energy E_a decreases with the gate voltage, which can be attributed to the decease of energy gap between the Fermi level, E_F, and conduction band edge, E_C, as the Fermi

level is tuned toward the conduction band by the gate voltage. E_a becomes flat with further increase of voltage indicates the minimum schottky barrier which can't adjust or alter by adjusting the gate voltage. The slope of the curves at low gate voltages (when the devices are in the fully depleted region) can be expressed as $dE_a/dV_{bg} = -dE_F/ dV_{bg} = -eC_{bg}/(C_{bg} + e^2D(E))$, where D(E) represents the density of trap states at the interface between the $MoSe_2$ channel and substrate. The density of trap states is found to be $\approx 7.6 \times 10^{12}$ and $\approx 4.9 \times 10^{12}$ cm^{-2} for $MoSe_2$ on SiO_2 and parylene-C, respectively, in excellent agreement with the reported D(E) of multilayer MoS_2 on SiO_2.[99] The rather similar D(E) for SiO_2 and parylene-C substrates further indicates that Coulomb impurities scattering is unlikely the limiting factor of the drastically different mobility in our $MoSe_2$ devices on SiO_2 and parylene-C.

4.4 SUMMARY

In conclusion, we characterized the $MoSe_2$ crystal by scanning tunneling microscopy (STM), fabricated few layer $MoSe_2$ FET devices on SiO_2 and parylene-C substrates and characterized their transport properties separately. The room temperature mobility of $MoSe_2$ FETs on parylene-C is significantly higher than that in $MoSe_2$ FETs on SiO_2.The mobility degradation on SiO2 substrate at room temperature is due to the extrinsic scatting primarily due to remote surface polar optical phonon scattering since the phonon excitation energy of SiO_2 is lower and can easily populated by room temperature thermal energy. On the other hand, optical phonon scattering from parylene-C is nearly absent because of its higher optical phonon energy which reduces the effect of phonon scattering and gives higher carrier mobility on parylene-C.

The mobility values of $MoSe_2$ devices both on SiO_2 and parylene-C converge at sufficiently low temperatures where acoustic phonons dominate. The stronger temperature dependence mobility on SiO_2 further suggests the optical phonon limited mobility. Some of the devices on SiO_2 show

the mobility saturation at low temperatures indicates the Coulomb scattering limited transport mechanism originated from $MoSe_2/SiO_2$ interface.

CHAPTER 5 FACILE 2D/2D MATERIALS VERTICAL VAN DER WAALS ASSEMBLY TO ACHIEVE LOW RESISTANCE OHMIC CONTACT

5.1 INTRODUCTION

A major challenge for developing TMDs-based electronic devices is to reduce the substantial Schottky barrier (SB) with most metals commonly used for making electrical contacts.[19, 100] But low resistance ohmic contacts are needed for exploring intrinsic transport properties of the channel material to find the performance limits of real device applications. So the fundamental question is how to achieve ohmic contact for TMDs-based semiconductor channel.

First approach to achieve low resistance contacts between a semiconductor and a metal lowering the SB height by selecting contact materials with an extremely high (for p-type semiconductors) or low (for n-type semiconductors) work function. If the metal work-function is close to the conduction band edge for n-type TMDs and valance band edge of p-type TMDs, low resistivity contacts are expected. It is extremely challenging to find metals with a proper high or low work function that also exhibit a high conductivity and chemical, thermal, and electrical stability. *Das et. al.* reported the variation of schottky barrier of MoS_2 metal junction by using available different work function metal.[100] In particular, a recent study shows that Fermi level pinning is present at the metal/TMDs contacts for a variety of metals with the work functions spanning a wide range which prevents the benefit of selecting proper work function for lowering the SB.[100, 101] Fermi level pinning drastically reduces the tunability of schottky barrier.[75]

The second approach is to heavily dope the source/drain regions of TMDs/metal contacts to thin the schottky barrier width. There are different doping methods such as solid doping, gas doping molecular doping, and chemical doping.[17, 92, 102-106]. However, doping methods are not

stable for long run. NO_2 and K doping is not stable in air. Indium adheres poorly to the substrate and is thermally unstable due to its low melting point of 156 °C.[19]Previously, we have reported significant improvement of electrical metal contacts in few-layer MoS_2 devices and graphene contact WSe_2 devices by drastically reducing the SB thickness using an ionic liquid (IL) gate.[92, 107] Ionic liquid is used to tune the contact as well as form electric double layers to form high capacitance for high tunability. But the ionic liquid is not stable at room temperature ambient condition and the improved charge injection efficiency using this method is still fundamentally limited by the height of the Schottky barrier of either the carriers. Recently low ohmic contact of metal TMDs is reported by phase engineering.[29, 106, 108] s stability with long term and introduction of foreign material during the phase change process limits its further applications. Besides this all efforts to reduce the metal TMDs schottky barrier for achieving ohmic contact is still challenging. Recently *Das et. al* presented the Nb-doped MoS_2 has negligible barrier with metal contacs.[109] This opens up the new strategy to overcome the significant TMDs metal barrier to achieve ohmic contact.

We proposed the doped (n or p) TMDs contact with pristine TMDs by van der Waals assembly of 2D crystals to achieve the ohmic contact. The pristine TMDs, which channel properties has to be study, make contact with substitutional doped TMDs and the doped TMDs connect to the metal. Metal and doped TMDs has negligible barrier. In this case, the substitutional doped TMDs act as drain/source electrodes of pristine TMDs. On the other hand, if the pristine TMDs and doped TMDs form ohmic contact then it is ideal to study the channel properties of undoped TMDs. The undoped TMDs can make hetero-junction or homo-junction depending upon the selection of TMDs to make contacts. For a vertical contact in TMDs, there are two barriers: vertical barrier at the contact due to van der Walls gap as mark A in **Fig. 5.1.1**

and horizontal barrier due to the doping difference as mark B in **Fig. 5.1.1**. For homo-junction, their Fermi levels close enough to align and form negligible barrier as shown in sketch of **Fig. 5.1.1**. But for hetero-junction, depending upon their Fermi levels alignment, it forms depletion barrier or accumulation barrier as shown in sketch **Fig. 5.1.1**.

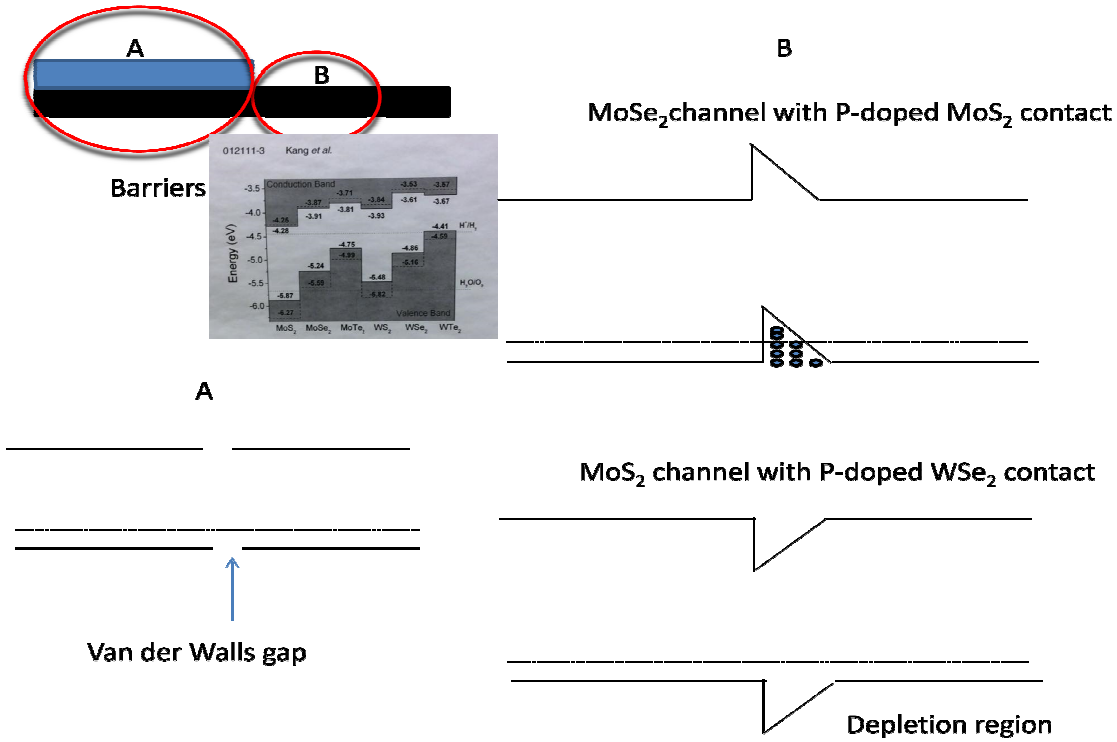

Fig. 5.1.1 Schetemic diagram of vertical and horizonatl barriers in TMDs/contact, TMDs 2D homo-junction barrier, TMDs 2D hetero-junction barrier with accumulation and depletion regions

5.2 EXPERIMENTAL DETAILS

The study the properties of van der Waals assembly of 2D materials is a interesting and doping level of these assembly added extra flavor to study the contact behavior according to doping concentration and contact materials combination. The contact might be assembly of same materials with different doping level (homo contact) or different materials of different doping concentration (hetero contact). To test the homo and hetero 2D TMDs contact behavior and its

feasibility as a low resistance ohmic contact, we made devices in four different combinations for hetero 2D contact and two different combinations for homo 2D contact as below:

5.2.1 TMDs HETERO CONTACT

We can transfer doped 2D TMDs contact with different materials than the channel material. Because of different materials on contact and channel, the combination form heterocontact.

(i) $MoSe_2$ with Nb-doped-MoS_2 contact

(ii) WSe_2 with Nb-doped-MoS_2 contact

(iii) $MoSe_2$ with Nb-doped-WSe_2 contact

(iv) MoS_2 with Nb-doped-WSe_2 contact

5.2.2 TMDs HOMO CONTACT

We can transfer 2D TMDs contact with doped same materials of the channel material. This type of combination is formed homo 2D contact.

(i) MoS_2 with Nb-doped-MoS_2 contact

(ii) WSe_2 with Nb-doped-WSe_2 contact

The undoped MoS_2 bulk crystal was bought from SPI supplies and $MoSe_2$ and WSe_2 crystals were are grown by chemical vapor deposition as described experimental section 4.2. 0.5% niobium (Nb) was doped on undoped MoS_2 (WSe_2) crystal to make p-doped crystal.

Thin h-BN flakes were produced by a repeated splitting of bulk crystals using a mechanical cleavage method on scotch tape. Poly-dimethylsiloxane (PDMS) gel was spin casted on silicon wafer at 400rpm for 30secs and kept on hot plate at 80℃ until 30 minutes and allowed to cool it down. The PDMS layer was cut it small pieces and gently transferred to scotch tape having thin flakes of h-BN getting from mechanical cleavage method from bulk crystal. Large, thin (10 - 50

nm), ultraclean wrinkle-free and smooth surface h-BN flakes were searched under optical microscope. The PDMS stamp having sample was gently pressed and transferred to clean glass slide and subsequently transferred on cleaned Si substrate with 270 nm $SiO_2$by home-built precision transfer stage. The h-BN flake surface was characterized by non-contact mode AFM to ensure it is ultraclean and smooth. Then the undoped TMDs were exfoliated to thin enough on scotch tape and transferred on PDMS. Thin (3 - 11 nm) flakes were searched by optical microscope and transferred on the top of smooth hBN which was already transferred on Si/SiO_2 substrate. Thin (10 - 50 nm), ultraclean wrinkle-free and smooth h-BN flakes were used to cover the central channel by leaving outer edge open on both sides **Fig. 5.2.1** in step 3. Now the Nb-doped TMDs were exfoliated on scotch tape transferred on PDMS stamp as described earlier. Thin (5 - 20 nm), ultraclean wrinkle-free and smooth surface Nb-doped TMDs flakes were identified by optical microscope and transferred on the both sides of the top h-BN to make contact on undoped TMDs as shown in **Fig. 5.2.1** in step 4 to make 2D homo (hetero) vertical contact. TMDs 2D contact FET devices were fabricated using standard electron beam lithography and deposited 10 nm of Ti and 40 nm of Au at ultra-high vacuum ($\sim 5x10^{-7}$torr). Complete process of fabrication of TMDs 2D contact FET is shown in figure **Fig. 5.2.1**.

Every step in the transfer process is crucial which can easily introduce impurities from PDMS stamp and form wrinkles during transfer process. To remove impurities and wrinkles during transfer process, the substrate was annealed at 400°C for 30 minutes in every steps of transfer. The substrate was annealed at 250°C for 30 minutes after transfer of TMDs flakes to minimize the thermal defects in TMDs channel. Non-contact mode AFM was used to determine dimensions and cleanness of the sample. Transport properties of the FET devices were measured by a Keithley 4200 semiconductor parameter analyzer in a Lakeshore Cryogenic probe station

under high vacuum (~ 1×10^{-6} torr) and in a Physical Property Measurement System (PPMS) from Quantum Design.

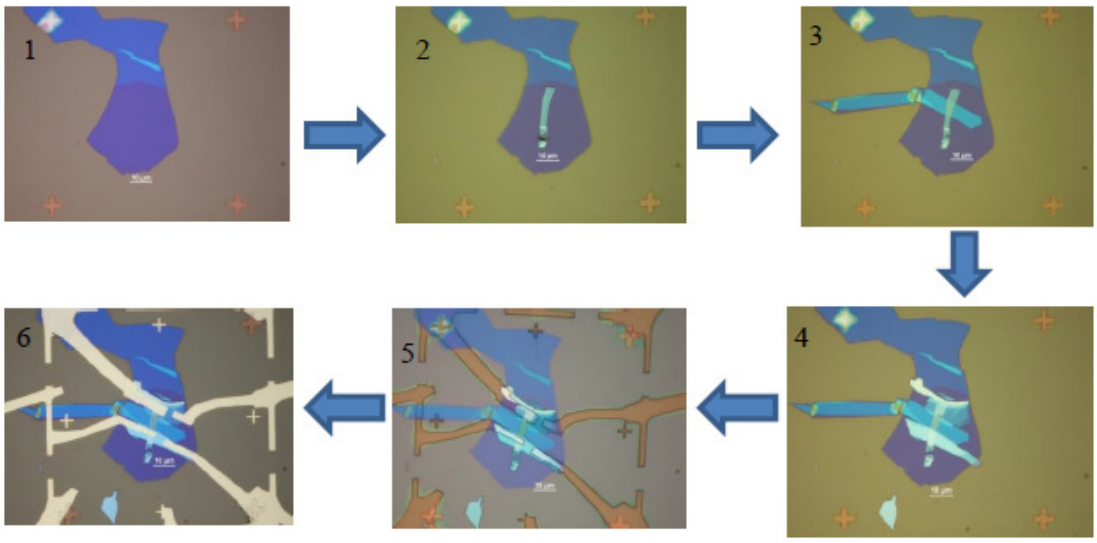

Fig. 5.2.1 Flow chart of fabrication process of TMDs 2D contact FET on h-BN

5.3 RESULTS AND DISCUSSION

Two of my colleagues are focused on TMDs 2D homo vertical contact and I am basically focused on TMDs 2D hetero vertical contact to get complete set of on this combination of FET devices.

The devices were classified into two categories, first set of TMDs 2D materials vertical contact having accumulation contact region: $MoSe_2$ with Nb-doped-MoS_2 contact and WSe_2 with Nb-doped-MoS_2 contact. Second set of TMDs 2D materials vertical contact having depletion contact region: $MoSe_2$ with Nb-doped-WSe_2 contact and MoS_2 with Nb-doped-WSe_2 contact.

First of all, we measured the I-V characteristics of first set of devices from room temperature to down 5K to verify the quality of contact. Both types of devices shows ideal linear behavoiur above the threshold voltage at all temperatures indicating nearly barrier-free ohmic contact. I-V characteristics of such devices are shown in **Fig. 5.3.1** (b), (c), (e) and (f) at temperatures 5K,

295K, 77K and 295K repectively. This indicates that the TMDs 2D verical junction is the promising mehod to eliminate the contact resistance by selecting appropriate doping contact and will turn to be universal contact to study the channel properties of TMDs.

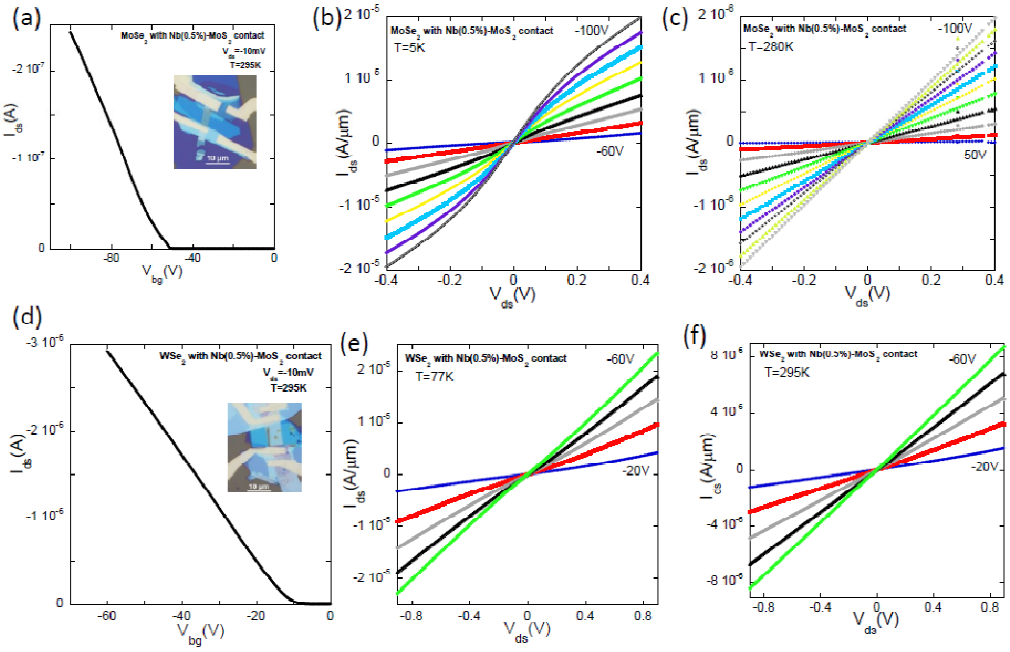

Fig. 5.3.1 (a) Transfer characteristics of $MoSe_2$ FET with Nb-doped (0.5%)-MoS_2 contact with V_{ds} = -10 mV at room temperature (in set:optical image of typical device) (b, c) Output characteristics of the device at 5K and 280K (d) Transfer characteristics of WSe_2 FET with Nb-doped (0.5%)-MoS_2 contact with V_{ds} = -50 mV at room temperature (in set:optical image of typical device) (e, f) Output characteristics of the device at 77K and 295K

We measured transfer curve of first set of FET devices ($MoSe_2$ with Nb-doped-MoS_2 contact and WSe_2 with Nb-doped-MoS_2 contact). They showed p-type behavior as shown in **Fig. 5.3.1** (a) and (d). **Fig. 5.3.1** (a) is transfer characteristics of $MoSe_2$ FET with Nb-doped (0.5%)-MoS_2 contact (V_{ds} = -10 mV) at room temperature (in set:optical image of device) and). **Fig. 5.3.1** (d) transfer characteristics of WSe_2 FET with Nb-doped (0.5%)-MoS_2 contact (V_{ds} = -50 mV) at room temperature (in set: optical image of device). The threshold voltage of $MoSe_2$ device is at ~ -50Vand the threshold voltage of WSe_2 device is at ~ -10V. The $MoSe_2$ devices shows larger negative threshold voltage than the WSe_2 devices as expected because of natural n-

doping on $MoSe_2$ channal. The on/off ratio of $MoSe_2$ device is > 10^8 order of magnitude and on off ratio of WSe_2 device is > 10^6 order of magnitude. We also determined the subthrold swing (SS) of $MoSe_2$ and WSe_2 devices which is one of the fundamental property to determine the better performance of TMDs FET. $MoSe_2$ FET with Nb-doped (0.5%)-MoS_2 contacts shows SS value 880 mV/dec and WSe_2 FET with Nb-doped (0.5%)-MoS_2 contacts shows SS value 790 mV/dec at room temperature. The on/off ratio and subthreshold swing of MoS_2 and WSe_2 devices are shown in **Fig. 5.3.2**.

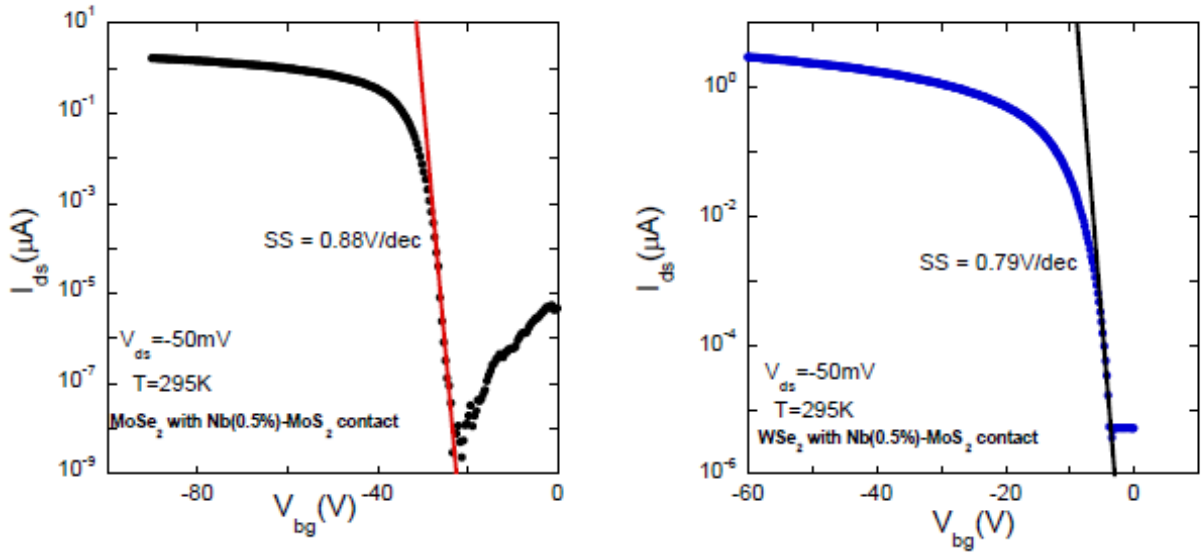

Fig. 5.3.2 Subthreshold swing (SS) of $MoSe_2$ FET with Nb-doped (0.5%)-MoS_2 contact and WSe_2 FET with Nb-doped (0.5%)-MoS_2 contact with V_{ds} = -50 mV at 295K

We further measured transfer characteristics from room temperature to 5K and extracted back gate dependence conductivity at different temperatures. **Fig. 5.3.3** (a) shows back gate dependence conductivity of $MoSe_2$ FET with Nb-doped (0.5%)-MoS_2 contact with V_{ds} = -10 mV at different temperatures from 2-probe measurements and **Fig. 5.3.3** (c) shows back gate dependence conductivity of WSe_2 FET with Nb-doped (0.5%)-MoS_2 contact with V_{ds} = -50 mV at different temperatures from 2-probe measurements.Clearly there are two regions for both types of devices, insulating or semiconducting section at low back gate with conductivity

increases with temperature and metallic section at high back gate with conductivity decreases with increase of temperature. The cross over from metallic to insulating region is consistent with metal-insulator transition (MIT) observed in TMDs as well as theoretical expectations for 2D semiconductors.[1112, 15] We extracted the temperature dependence 2-probe field effect mobility from the conductivity curve. 2-wire field effect mobility of $MoSe_2$ FET is extracted at back gate voltage region $-70V < V_{bg} < -100V$ of conductivity curve and that of WSe_2 FET is extracted at back voltage region $-40V < V_{bg} < -60V$ of WSe_2 conductivity curve. The temperature dependence mobility increases monotonically with decrease of temperature. **Fig. 5.3.3** (b) and (d) show the temperature dependence 2-wire field effect mobility of $MoSe_2$ FET and temperature dependence 2-wire field effect mobility of WSe_2 FET. In inset log-log plot of 2-probe field effect mobility is shown. The mobility of all the devices lies between 100 $cm^2V^{-1}s^{-1}$ to 150 $cm^2V^{-1}s^{-1}$. The 2-wire field effect mobility of $MoSe_2$ FET with Nb-doped (0.5%)-MoS_2 contacts is over 2600 $cm^2V^{-1}s^{-1}$ at 5K with is record high two-wire field effect mobility at this tmperature.[110]

Now we chose the second set of TMDs 2D materials vertical contact having depletion contact region: $MoSe_2$ with Nb-doped-WSe_2 contacts and MoS_2 with Nb-doped-WSe_2 contacts. First of all, we measured the I-V characteristics of first set of devices from room temperature to down to verify the quality of contact. Although both types of devices showslinear current-voltage relation at room temperature, non-linear I-V behavoiur is obsreved even above the threshold voltage below the temperatures indicating contacts are limited by barrier. I-V characteristics of $MoSe_2$ with Nb-doped-WSe_2 contact are shown in **Fig. 5.3.1** (a) and (b) at temperatures 295K, and 77K repectively. Furthermore, MoS_2 with Nb-doped-WSe_2 contacts FET has even larger rectifying contact. This indicates that the TMDs 2D verical junction with depletion contact has huge barrier. We further measured temperature dependence transfer characteristics and extracted

back gate dependence conductivity at different temperatures. **Fig. 5.3.4** (c) shows back gate dependence conductivity of $MoSe_2$ FET with Nb-doped (0.5%)-WSe_2 contact with V_{ds} = -50 mV at different temperatures from 2-probe measurements and **Fig. 5.3.4** (d) shows back gate dependence conductivity of MoS_2 FET with Nb-doped (0.5%)-WSe_2 contact with V_{ds} = -50 mV at different temperatures from 2-probe measurements. Unlike first type of devices, the threshold hold voltage shifts to furher negative with decreease of temperature without showing transition of insulating regin to metallic region. This indicates the contacts form significant barrier for charge carriers. The Nb-doped (0.5%)-WSe_2 contacts form depletion barrier with MoS_2 and $MoSe_2$ channels which creates significant barrier for holes. At room temperature the carriers may cross the barrier depending upon barrier height but at low temperature the carries which can cross the barrier significantly reduced.

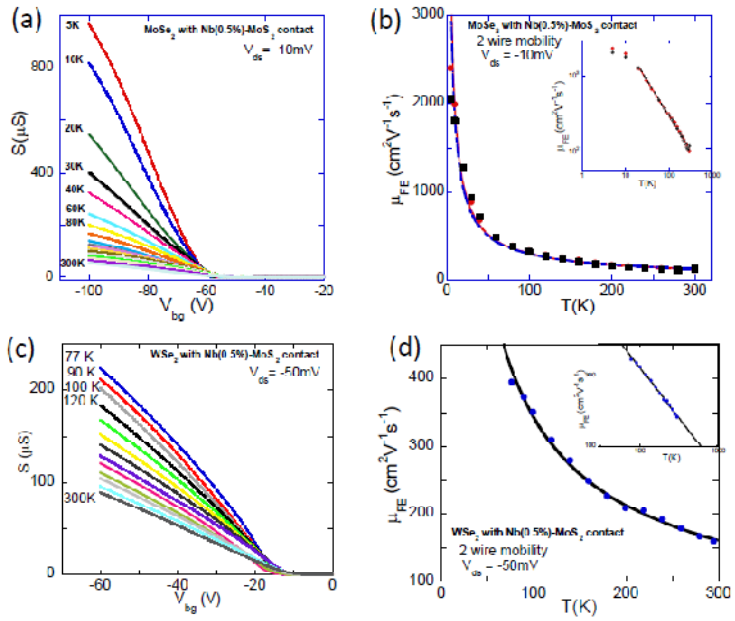

Fig. 5.3.3 (a) Back gate dependence conductivity of $MoSe_2$ FET with Nb-doped (0.5%)-MoS_2 contact with V_{ds} = -10 mV at different temperatures (b) Temperature dependence 2-wire field effect mobility of $MoSe_2$ FET with Nb-doped (0.5%)-MoS_2 contact with V_{ds} = -10 mV extracted at -100V < V_{bg}< -70V (inset: log-log plot) (c) Back gate dependence conductivity of WSe_2 FET with Nb-doped (0.5%)-MoS_2 contact with V_{ds} = -50 mV at different temperatures (d) Temperature dependence 2-wire field effect mobility of WSe_2 FET with Nb-doped (0.5%)-MoS_2 contact with V_{ds} = -50 mV extracted at -60V < V_{bg}< -40V(inset: log-log plot)

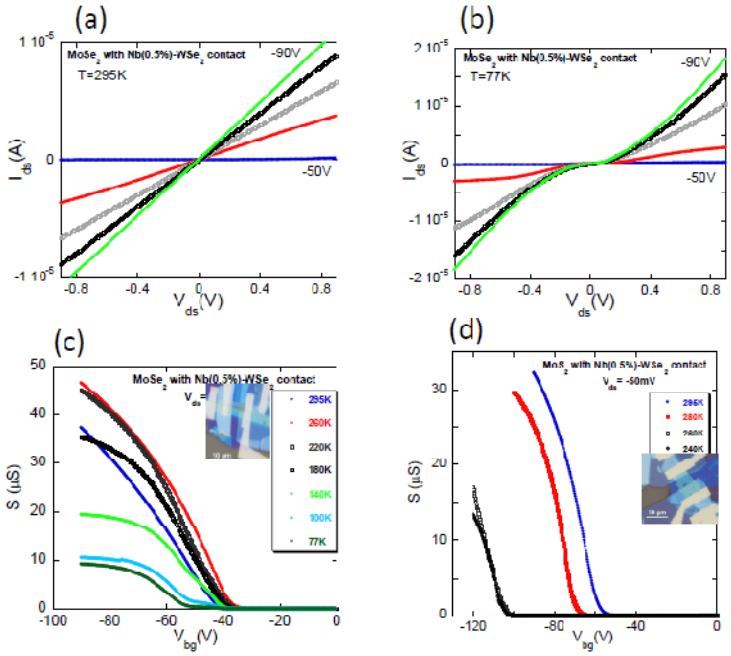

Fig. 5.3.4 (a, b) Output characteristics of $MoSe_2$ FET with Nb-doped (0.5%)-WSe_2 contact at 295K and 77K (c) Back gate dependence conductivity of $MoSe_2$ FET with Nb-doped (0.5%)-WSe_2 contact with V_{ds} = -50 mV at different temperatures (d) Back gate dependence conductivity of MoS_2 FET with Nb-doped (0.5%)-WSe_2 contact with V_{ds} = -50 mV at different temperatures

5.4 SUMMARY

In summary, we have developed a novel 2D/2D contact strategy for van der Waal assembly of 2D layer TMDs. We further study the different mechanisms of hole carrier injection along the contact of 2D/2D van der Waals assembly by characterizing their transport properties. We developed facile new approach to achieve high-quality ohmic contacts for MoS_2, $MoSe_2$ and WSe_2 FETs by designing homo and hetero van der Waal stacking for possible 2D TMDs combination of their doped and undoped crystal. The low-resistance contacts lead to improved device performance, including high on/off ratios, high drive currents, and record high two-terminal field effect mobility at cryogenic temperatures. The van der Waal stacking approach for contact engineering is applicable to a wide range of 2D materials for both *p*-type and *n*-type transistor and expected to compatible for production of flexible electronics.

CHAPTER 6 STUDY THE FUNDAMENTAL PROPERTIES OF BLACK PHOSPHORUS

6.1 INTRODUCTION

Two dimensional (2D) layered materials have become one of the most attractive materials for electronics and optoelectronics applications due to their unique properties such as chemically & thermally stable, mechanically flexible & strong, structure stability, surface smoothness and absence of dangling bonds.[1-3] Graphene has shown extremely high mobility, optical transparency, and broadband absorption.[65-69] However, graphene has zero band gap and photoexcited electron–hole pairs recombine extremely fast which limit graphene's potential in digital electronic applications and photovoltaic generation.[70, 71] 2D transition metal dichalcogenides (TMDs) like MoS_2, $MoSe_2$ WSe_2etc show very high on/off current ratios with graphene like properties, but their relatively low carrier mobility and sizeable band gap (>1 eV) limit their applications in electronics and optoelectronics.[101, 111-115] Recently, a new class of 2D layered material, phosphorene or few-layer black phosphorus (BP), has attracted particular attention to researchers. It shows excellent transistor performances as comparable to TMDs FETs withits carrier mobility is significantly higher than that of TMDs.[35, 116, 117] The band gap of bulk BP is 0.3 eV, while its few-layer structures have thickness-dependent direct band gaps ranging from 2 eV to 0.3 eV,[31-34] opening up new opportunities for electronic and optoelectronic applications. In contrast to TMDs, few layers BP has direct band gap. In addition, the electrical and optical conductivities of BP show anisotropic mechanical, thermal, electrical and optical properties unlike other 2D materials.[32, 35, 36] The BP easily reacts with air in presence of water vapor which degrades its electrical properties gradually. The degradation enhances in presence of light.[37] This property of BP challenges the researchers to prevent to contact with air, water and light for preserving it pristine properties.

6.2 FABRICATION PROCESS

BP crystal which kept in high vacuum to prevent degradation by ambient condition was taken out and split it into small crystal by tweezers. The small crystal from the inner side of the bulk crystal was kept in scotch tape. Ultrathin BP crystals were produced by repeated splitting of the crystals using a mechanical cleavage method and eventually transferred to degenerately doped silicon substrates covered with 290 nm SiO_2.[8] Optical microscopy was used to identify thin BP crystals and non-contact atomic force microscopy (AFM) was used to further characterize. We chose 3nm to 15 nm of BP crystal for device fabrication because multilayer BP of this thickness range has a much high yield of sufficiently large flakes (for patterning multiple electrodes) and less susceptible to surface oxidation in ambient conditions compared to thinner samples, while still maintaining a reasonably large on/off ratio for FET operations. The BP thin flakes were searched and characterized quickly and spin casted PMMA as a passivation layer to avoid ambient oxidation of BP flake surface. BP FET devices were fabricated using standard electron beam lithography and developed was not done until e-beam metal evaporator is ready. After developed, the substrate was quickly kept in BJD-1800 chamber at high vacuum to deposit metal. Electron beam deposition of 5 nm of Ti and 40 nm of Au was done at ultra-high vacuum (~$5x10^{-7}$ torr). To eliminate electrical contact contributions, we also patterned voltage probes in between drain and source electrodes to facilitate four-terminal measurements. An optical micrograph of a typical BP device is shown in the inset of **Fig. 6.3.2 (a)** inset. After lift-off, the device was immediately kept in cryogenic ultrahigh vacuum chamber for transport measurements. To test the anisotropic transport and optical properties of black phosphorous crystal, drain source electrodes are defined in mutually perpendicular direction of a sample and measured device properties separately.

6.3 RESULTS AND SISCUSSION

6.3.1 SCANNING TUNNELING MICROSCOPY STUDY OF BLACK PHOSPHORUS CRYSTAL

First of all, BP crystal was freshly cleaved inside an ultra-high vacuum chamber at room temperature to avoid degradation and placed in a microscope stage overnight at 80 K. Scanning tunneling microscopy (STM) measurements are performed on cleaved surfaces of BP crystals to characterize quality of the crystals. **Fig. 6.3.1 (a)** shows a STM topographic image of a BP crystal surface, where distinct defects are clearly visible in addition to an atomic-flat cleaved plane. Such defects appeared at the fresh-cleaved surface, indicate impurities of BP crystals. Since defects and/or impurities enhance scattering of charge carriers and thus mobility is severely reduced. In order to achieve the ultimate device performance, extremely low impurity level and high crystalline quality is required. **Fig. 6.3.1 (b)** shows anatomic resolution topographic STM image of BP crystals on the clean flat area of BP surface marked as rectangle in **Fig. 6.3.1 (a)**. As described in the puckered-layer model, an upper phosphorus atom sits just directly above a lower one. Since STM is a surface-sensitive technique, we can assign easily the bright spots in this atomic-resolved image to the upper phosphorus atoms. Therefore, only zigzag atomic chains composed of the upper atoms are visible in the STM image of BP surface. A close-up image in **Fig. 6.3.1 (c)** shows more highly resolved features of the surface structure. As shown in the atomic model, all surface phosphorus atoms almost reside in their original sites and surface reconstruction is not observed. The in-plane lattice constants "a_x" (along the direction of a lighter effective mass) and "a_y" (along the direction of a heavier effective mass) measured from the STM image are 4.4 Å and 3.4 Å, respectively, which is in good agreement with the reported values of bulk BP.[31, 33, 34] Our STM observation agrees very well with the previous reported STM work on BP crystal.[118]

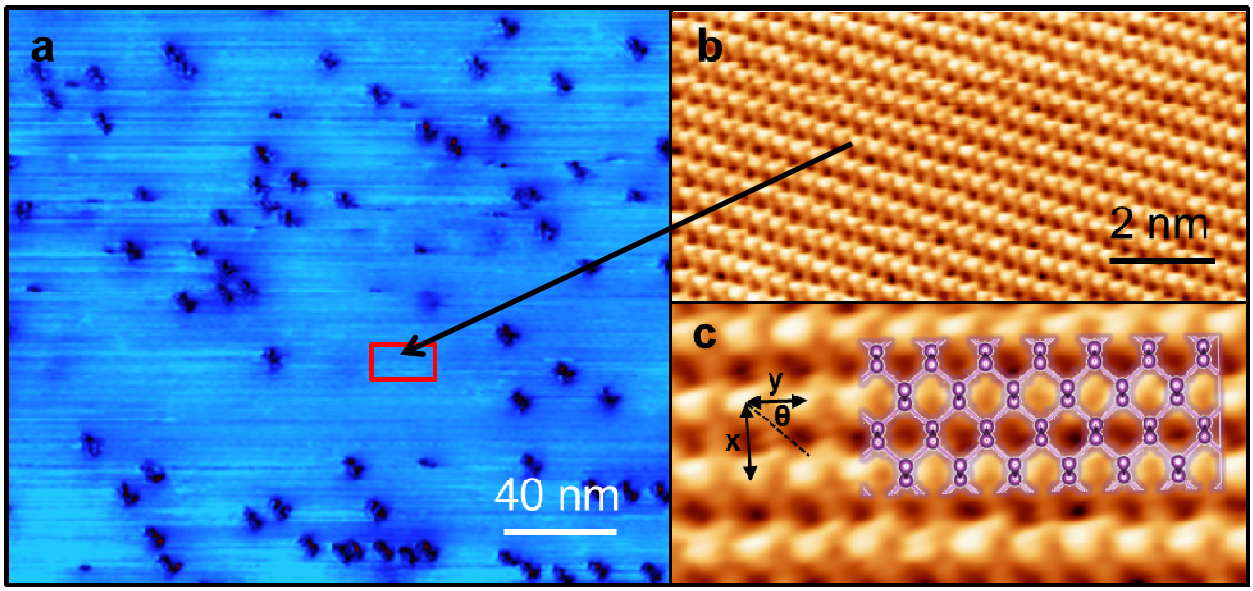

Fig. 6.3.1 STM images of BP crystals. (a) STM topographic image of a freshly cleaved BP surface with scan size of 240 nm x 240 nm; (b) a zoom-in image of BP with atomic resolution into the flat area marked by rectangle in (a); and (c) a close-up image showing detailed features of the BP surface structure along x and y directions. θ is defined as the angle between a specific direction (dashed line) and the y-axis.

6.3.2 AMBIENT DEGERATION TEST OFBLACK PHOSPHORUS

Before start to making BP FETs, we studied its surface oxidation in ambient condition with variation of humidity. The BP flakes were exposed in air and took it topographic image by AFM. We clearly saw the bubble like structure on the surface of BP indicating surface oxidation. The size and density of the bubble depends up on the ambient exposure time, humidity of lab and presence of light. More exposure time increases the bubble density and size suggesting the more BP atoms oxidize. We observed increase rate of oxidation in presence of light and higher humidity level. **Fig. 6.3.2** (a) shows the representative AFM topographic image of BP flakes after 3 hours exposure in air. It clearly shows the highly dense humps with thickness from couple of nanometer to 12 nm. On the other hand, The BP thin flakes were transferred quickly and spin casted PMMA as a passivation layer to avoid ambient oxidation of BP flake surface. BP FET was designed by standard e-beam lithography. The FET was developed and quickly put in BJD-

1800 chamber at ultrahigh vacuum and deposit Ti/Au. The device was lift of and characterized immediately by AFM. **Fig. 6.3.3** (a) shows the AFM topographic image of part of BP FET making by spin casting PMMA immediately after flake. The surface of BP is smooth and bubble free suggesting no oxidation. This method was adopted to make BP FETs throughout our measured devices to test pristine ultrathin BP flakes properties.

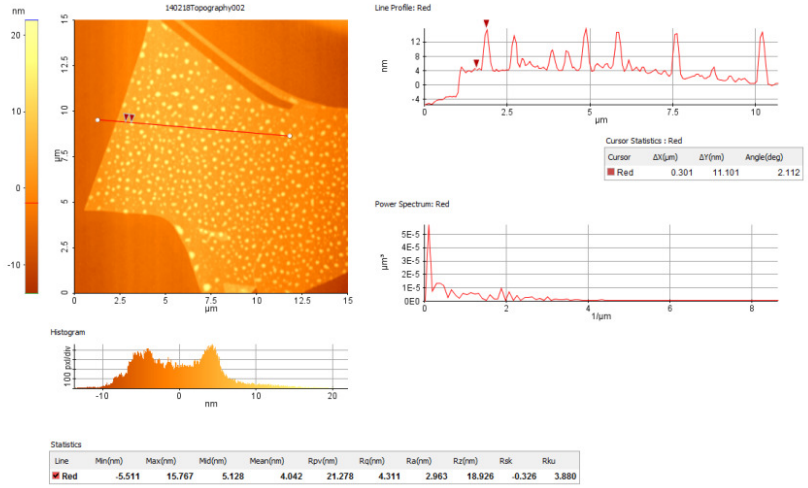

Fig. 6.3.2 (a) AFM topographic image of BP flakes after 3 hours exposure in air

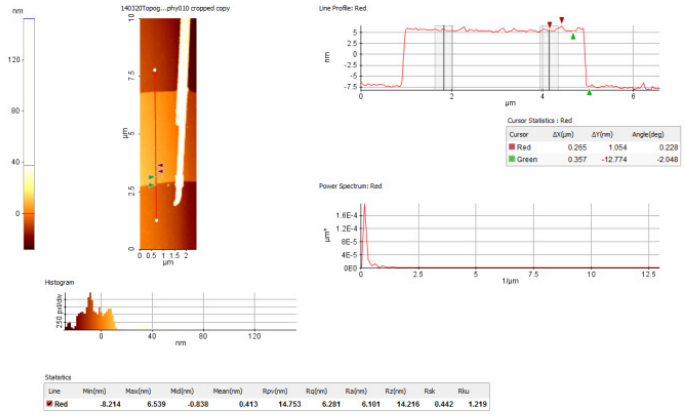

Fig. 6.3.3 (a) AFM topographic image of part of BP FET making by spin casting PMMA immediately after flake was made to minimize exposure in air

6.3.3 TRANSPORT PROPERTIES BLACK PHOSPHORUS FIELD EFFECT TRANSISTOR

The BP thin flakes were transferred quickly ON Si/SiO_2 substrate and spin casted PMMA as a passivation layer to avoid ambient oxidation of its surface. BP FETs were designed by standard e-beam lithography. The FET was developed and quickly put in BJD-1800 chamber at ultrahigh vacuum and deposit Ti/Au. The FET is immediately kept in high vacuum cryogenic probe station after lift to study its transport properties. The steps and time are important to avoid surface oxidation of black phosphorus.

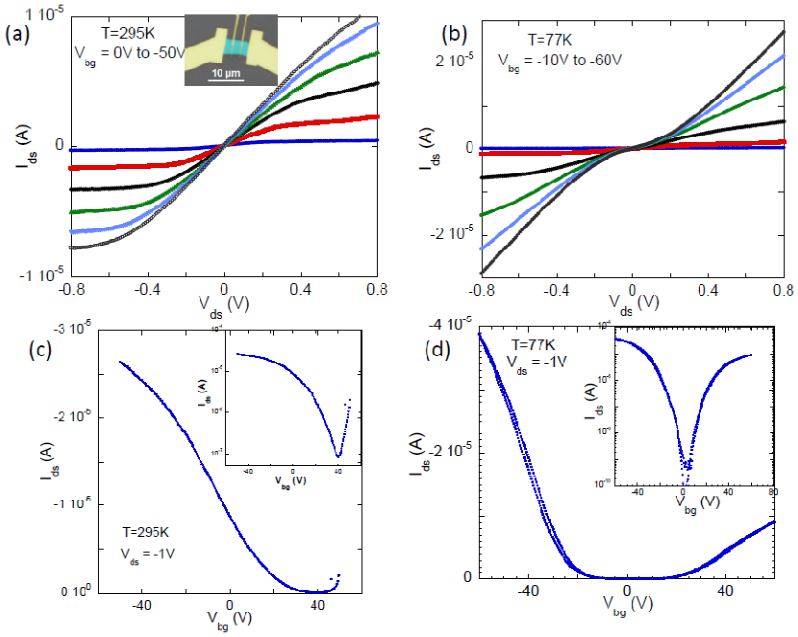

Fig. 6.3.4 (a, b) Output characteristics of 13.0 nm BP FET at 295K and 77K respectively (c, d) transfer characteristics of BP FET at 295K and 77K respectively with semi-log plot in inset

First of all, we measured the output properties of BP FETs to test the quality of metal contact. **Fig. 6.3.4** (a) and (b) show the output characteristics of BP FET at 295K and 77K respectively. It shows linear I-V characteristics at high gate voltage (V_{bg} > -20V) with saturation of current at high bias voltage at room temperature and slight non-linear at 77K, may be caused by slight surface oxidation during fabrication process. This observation is in qualitatively

agreement with the previously reported current saturation behavior in BP FETs.[116] The current saturation is likely caused by the reduction of the effective V_{bg} and V_{ds} due to the relatively large parasitic series drain/source contact resistance (R_C) given by $V_{bg\_eff} = V_{bg} - R_C I_{ds}$ and $V_{ds\_eff} = V_{ds} - 2R_C I_{ds}$.[19] Then, we measured the electrical transfer properties of BP FETs.**Fig. 6.3.4** (c) and (d) shows the transfer characteristics of a representative BP FET at room temperature and 77K with semi-logarithmic scales in inset. The device exhibits a predominately *p*-type behavior, with the on/off current ratio achieving more than $10^3$with a drain-source voltage of -1V at room temperature.

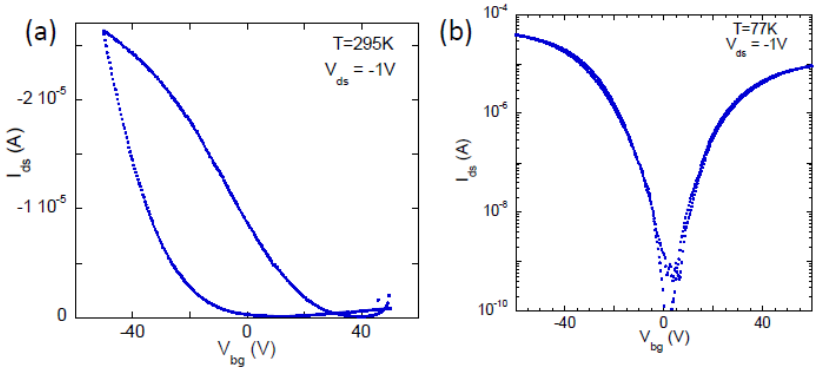

Fig. 6.3.5 Hysteresis of output characteristics of 13.0 nm BP FET at (a) 295K and (b) 77K respectively

We measured the duel sweep to monitor the hysteresis of transfer curve which indicates relatively large hysteresis at room temperature. The large hysteresis in the transfer characteristics is likely due to charge transfer from neighboring adsorbates (such as moisture and oxygen) or charge injection into the trap sites on the SiO_2 substrate and/or the surface oxidation layer of BP.[93, 117, 119] When the back gate voltage is swept toward the negative direction, a portion of the gate-induced holes are transferred to adsorbates, the surface oxidation layer and/or the substrate to fill the trap sites, leading to a slower rate change of the hole density in the channel (thus a

reduced transconductance dI_{ds}/dV_{bg}). The scenario reverses when the gate voltage is swept toward the positive direction.

To extract the conductivity, four probe gate dependence drain-source current is measured at low drain source bias voltage V_{ds} = -50 mV. The field-effect mobility was calculated by using standard formula $\mu = \frac{L}{W} X \frac{d\sigma}{dV_{bg}} X \frac{1}{C_{bg}}$, where L and W are length of inner probes and width of sample, σ is four probe conductivity, V_{bg} is back gate voltage applied, C_{bg} is geometrical capacitance. As a result of large hysteresis observed, the field-effect mobility estimated strongly depends on the gate sweep direction. The two probe field-effect mobility extracted from the positive gate sweep direction (103 $cm^2V^{-1}s^{-1}$) being nearly 3 times larger than that extracted from the negative gate sweep direction (38 $cm^2V^{-1}s^{-1}$) of a representative BP FET and other BP FET devices show similar result. To estimate $d\sigma/dV_{bg}$, we chose the linear region of the σ-V_{bg} curve and C_{bg} ≈1.2×10^{-8} F/cm^{-2} is the capacitance of the Si back gate. To investigate the channel-limited mobility, we also measured the back gate dependence of the conductivity in a four-terminal configuration at different temperatures. Our four-terminal conductivity measurement suggests a mobility improvement from 38 $cm^2V^{-1}s^{-1}$ to 52 $cm^2V^{-1}s^{-1}$ for the negative gate sweep direction. In addition to the defects and/or impurities in the BP crystals (as shown in **Fig. 6.3.1**), other factors such as the surface oxidation and non-ideal BP/dielectric interface may also degrade the mobility. We also know that the electrical conductivity of BP crystals is anisotropic. The carriers mobility along the x-direction (lighter effective mass) is 1.5-1.8 times higher than that along the y-direction (heavier effective mass), as reported in previous literatures.[35, 116] It is worth to note that our transport measurement is taken along the y-direction (heavier effective mass), which can be concluded from later photocurrent measurements. Although, the field-effect mobility observed in this device is significantly lower than the mobility values for bulk

phosphorus crystals, it is comparable to those reported for few nanometer thick BP crystals.[34, 35, 117]

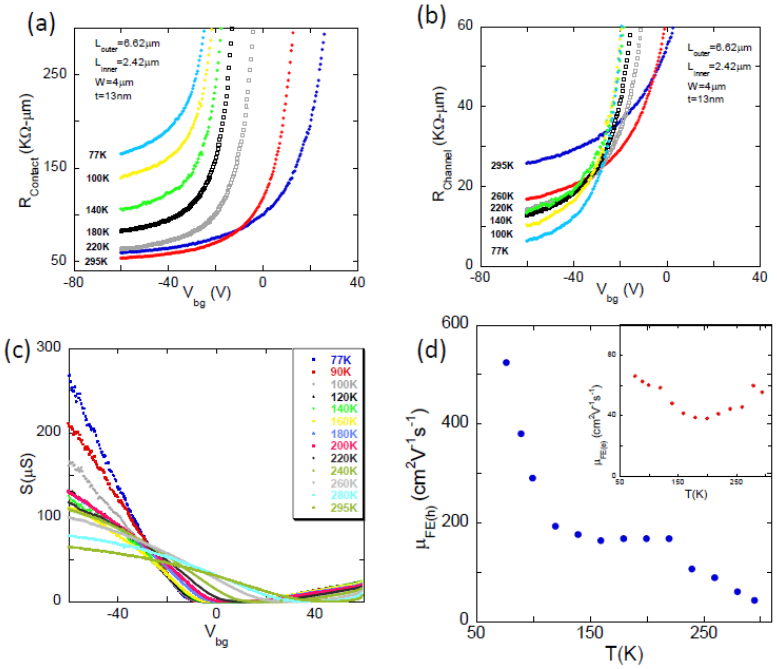

Fig. 6.3.6 (a) back gate dependence contact resistance of 13.0 nm BP FET at different temperatures (b) back gate dependence channel resistance of BP FET at different temperatures (c) Gate dependence 4-probe conductivity at different temperature of holes of BP FET (d) Temperature dependence 4-probe field effect mobility of holes of BP FET and its temperature dependence 4-probe field effect mobility of holes in inset

The contact resistances were estimated from four probe measurements. As shown in **Fig. 6.3.6** (a), the contact resistance estimated as $R_c = [(V_{ds}/I_{ds} - R_{ch})/2]$xW increases from ~50 KΩ·μm at V_{bg} = -60 V to over 90 KΩ·μm at V_{bg} = 0 V at room temperature, where V_{ds}/I_{ds} is the total resistance of the device and R_{ch} is the channel resistance extracted from the four-terminal measurements. Such a large contact resistance is expected to considerably reduce V_{bg_eff} and V_{ds_eff}, especially at low V_{bg} and high V_{ds} (e.g.V_{bg} = -20 V and V_{ds} = -1 V), where the voltage drop at the contacts ($R_C I_{ds}$ for V_{bg} and $2R_C I_{ds}$ for V_{ds}) is most significant. At high V_{bg} and low V_{ds}, $R_C I_{ds}$ is relatively small compared to the applied V_{bg} and V_{ds}, leading to nearly linear I_{ds}-V_{ds}

characteristics.[77] In addition to the presence of a Schottky barrier, possible sample surface oxidation during fabrication process may also contribute to the large contact resistance.[35, 117]

Fig. 6.3.6 (b) shows the gate dependence channel resistance at different temperatures of BP FET extracted from four terminal measurements which clearly shows two regions. At more negative back gate region, the channel resistance at low temperature is lower than its value at high temperature showing metallic behavior. But at low negative back gate region, the channel resistance at low temperature is higher than at high temperature region suggesting insulating behavior. Such metal to insulator transition is also observed temperature dependence hole conductivity curve as shown in **Fig. 6.3.6** (c). The 4 –probe field-effect mobility was calculated by using standard formula $\mu = L/W \times d\sigma/dV_{bg}/C_{bg}$ from the gate dependence conductivity curve at high negative gate voltage region. The temperature dependence mobility of hole is shown in **Fig. 6.3.6** (d). The mobility of hole increases with decreases of temperature suggesting phonon limited channel mobility of hole. On the other hand, the mobility of electron is calculated ~45 $cm^2V^{-1}s^{-1}$ which is almost constant at all temperature suggesting the electrons carrier is largely limited by schottky barrier.

6.3.4 BLACK PHOSPHORUS MOLYBDENUM DISULFIDE JUNCTION DIODE

Heterostructures based on two-dimensional (2D) materials have evolved exciting research field. Two dimensional materials have covalent bonds in-plane and van der Waals bonds between planes. So, when one type of 2D material comes into another type of 2D material, which enable the artificial stacking of 2D crystals on top of each other without the constraint of atomic commensurability. By choosing 2D materials with different band gaps and work functions, vertical integration of layered materials heterostrectures with tunable carrier concentrations can open up new device platform for future optoelectronic devices such as

photovoltaics, light-emitting diodes, and photodetectors.[120-12459, 120] Recently it is shown that the van der Waals heterostructures consisting of transition metal dichalcogenides (TMDs) are ideal candidates due to their unique optical properties and strong light-material interactions.[1, 125-128]2D p-n heterojunctions can be realized by simply stacking two TMD materials together.[59, 129-131] Unlike the conventional chemically doped p-n homojunctions, this 2D p-n heterojunctions provide an ideal ideality factor while concerns of lattice mismatches between materials are eliminated.[132]Black phosphorous (BP) has been demonstrated as another class of 2D material for electronics and optoelectronics.[38, 133-135] Bulk BP has a band gap 0.3 eV and few-layers BP have a thickness-dependent direct band gap ranging from 0.3 eV to 2 eV. The vertical heterojunction of TMDs and BP offers new possibilities for designing p-n junction semiconductor devices. BP is p-type semiconductor and MoS_2 is n-type semiconductor. It is worth to investigate the p-n junction device performance by stacking BP and molybdenum disulfide (MoS_2) as vertical p-n junction.

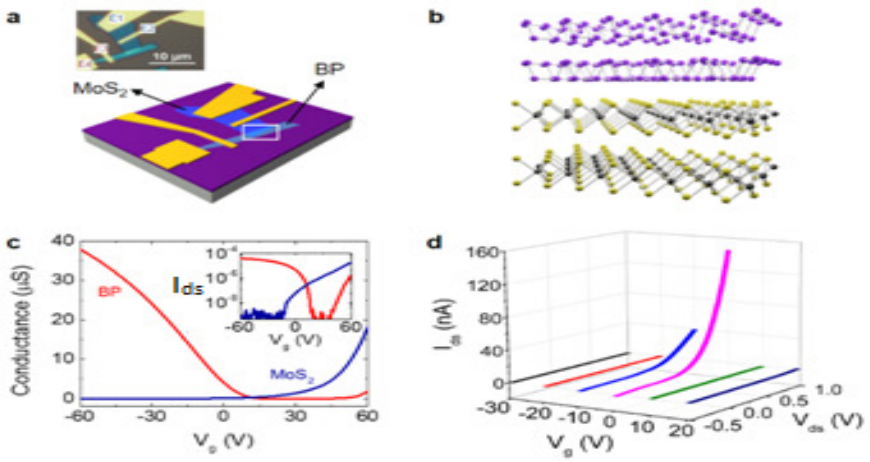

Fig. 6.3.7 (a) Schematic illustration of a BP-MoS_2 p-n junction with optical image of the junction on the top (b) Schematic illustration of the crystal structure of the junction(c) Gate-dependent transport characteristics for 8.0 nm BP (red curve) and 5.0 nm MoS_2 (blue curve) at V_{ds} = 100 mV, respectively. Inset: the same gate-dependent transport characteristics in a semi-log plot. (d) I-V curves at various gate voltages measured MoS_2-BP p-n junction.

Few layers MoS_2 flakes were prepared on scotch tape from bulk crystal by mechanical cleavage method and transferred on PDMS patch. The PDMS patch with MoS_2 was put on glass slide and made ready to transfer. BP flakes were transferred on Si/SiO_2 substrate and quickly scanned by optical microscope to find few layer better flakes. To make vertical MoS_2 and BP p-n junction, the MoS_2 on PDMS patch was immediately transferred on the target BP sample home-built precision transfer stage. PMMA was spin casted immediately to prevent oxidation of BP. Electrodes were defined by standard e-beam lithography with subsequent deposition of 5nm Ti and 40 nm Au. To measure MoS_2 and BP properties, two pairs of separate electrodes were designed to MoS_2 and BP separately. The inner pair of electrodes, one on BP and another on MoS_2 were used to study the MoS_2-BP p-n vertical junction properties. We measure the electrical property of the junction in high vacuum (~ 10^{-6}torr) with the gate voltage applied to the Si substrate to adjust the carrier concentration in each material. **Fig. 6.3.7**(a) shows the typical design of MoS_2-BP p-n vertical junction and device optical image on the top.

First of all, we measured the transfer characteristics of BP and MoS_2 devices separately to test their quality. At zero gate bias, BP shows typical p-type behaviour and MoS_2 shows n-type behaviour forming a p-n junction in the overlap region as expected. **Fig. 6.3.7** (c) shows gate-dependent transfer characteristics of BP (red curve) at V_{ds} = -100 mV and MoS_2 (blue curve) at V_{ds} = 100 mV, respectively with semi-log plot in inset. As the gate voltage increases to 60V, the BP crystal becomes n-doped whereas the MoS_2 layers become an elevated electron concentration. The I-V characteristics of the BP-MoS_2 p-n junction were measured at various gate voltages. Consistent with the gate-tuneable transport curves, the unintentional doping at zero gate bias allows for strong rectification of drain current. This rectification ratio reduces when the carrier concentrations in the

junction region are electrostatically modified. Although the observed I-V characteristics are similar to conventional p-n junctions, the electronic tunability of vertical p-n heterostructures are likely to be attributed to tunnelling-assisted interlayer recombination due to their absence of depletion region.[125] Details of the device characteristics with photo current measurement is reported in *Nanoscale* in 2015.[136]

CHAPTER 7 DIELECTRIC INTEGRATION

7.1 INTRODUCTION

Si substrates with thermally grown 290 nm or 270 nm SiO_2were used to study the fundamental transport mechanisms of TMDs FET devices which described in previous chapters. Other dielectric materials like Al_2O_3, h-BN transferred on Si/SiO_2 substrates to fabricate TMDs FET devices and measured in back gate configuration. The thicker dielectrics in back gate configuration requires large operating gate voltage to tune the channel which limits it practical applications. Adequate decrease of the dielectric thickness is one of the methods to decrease the operating voltage but the decrease of dielectric thickness causes different problems including gate leakage current, high power consumption also hard to control surface quality. On the other hand, the size of the transistor is equally important for high demand of miniaturization of electronic devices. Continuous miniaturization of electronic devices causes the short channel effect which caused by the encroachment of electric field from drain and source electrodes. Use of high-k dielectric as a gate dielectric help to prevents the short channel effect as discussed in chapter 1 as well as decrease the gate leakage current. **Table 7.1.1** shows the most commonly used dielectrics for CMOS applications with dielectric constant, band gap and crystal structure. The performance of the 2D electronic devices is affected directly and indirectly by dielectric surface properties and surface chemistry. So the selection of dielectric to integrate with 2D electronic devices is crucial. High-k dielectric is essential to screen the coulomb scattering as well as to reduce the short channel effect. Different high-k dielectrics are used in TMDs based electronics including Al_2O_3, HfO_2deposited by atomic layer deposition (ALD) technique. Atomic layer deposition (ALD) is the common practice to deposit high-**k** dielectrics on the surface of 2D layer semiconductors.[137-139] One of the difficult challenges scientific communities are struggling

is to deposit high-quality high-**k** dielectrics on the top surfaces of 2D layer semiconductors such as MoS_2, graphene because of the unsaturated bonds out of planes of layer materials. Different chemical treatment, UV and ozone exposure on the MoS_2 surface are the successful methods to functionalize the inert MoS_2 surface for ALD process. [140-142] Low-temperatures ALD grown by chemical treatment on the MoS_2 surface raises concerns of high levels of impurities, such as OH and C residues in the dielectric film and MoS_2 surface, as well as the repeatability of the process is main issue.[143, 144] This effect clearly degrades the electrical properties of ultrathin TMDs channel. UV exposure on the MoS_2 surface to functionalize the surface by oxygen adsorption to deposit high-κ could affect the optical and electrical properties of MoS_2.[145] The effort to functionalize the MoS_2 surface to deposit high-k dielectrics causes the severe changes of MoS_2 properties.[141-145] To overcome these difficulty we proposed new facile approach to get high-κ dielectric by thermal oxidation of 2D metallic layered TMDs. First, we prepared the TaS_2 ultra-thin and ultra-smooth flakes by mechanical exfoliation method from commercially available 1T TaS_2 crystal. The flakes were oxidized as described in method section.

Material	Dielectric constant	Band gap (eV)	Crystal structure
SiO_2	3.9	8.9	Amorphous
Al_2O_3	9	8.7	Amorphous
TiO_2	80-100	3.5	Tetragonal
Ta_2O_5	26	4.5	Orthorhombic
HfO_2	25	5.7	Monoclinic, tetragonal, cubic
ZrO_2	25	7.8	Monoclinic, tetragonal, cubic
Y_2O_3	15	5.6	Cubic
La_2O_3	30	4.3	Hexagonal, cubic
MgO	9.8	7.3	Cubic
Si_3N_4	-	-	Amorphous
Er_2O_3	14.4	7.5	-

PrO_2	25	3-4	Cubic
Parylene-C	3.5	-	Amorphous
Gd_2O_3	24	-	-
$ZrSiO_4$	-	-	Amorphous
$HfSiO_4$	-	-	Amorphous

Table 7.1.1 Some of the possible high – κ dielectrics with their dielectric constant, band gap and crystal structure[146]

7.2 EXPERIMENTAL DETAILS

7.2.1 C-V MEASUREMENT DESIGN

For capacitance-voltage (C-V) measurement, MIM junctions were designed by sandwiching an ultrathin Ta_2O_5 between a pair of metal electrodes. First, bottom electrodes consisting of 10 nm of platinum (Pt) with 5 nm of titanium (Ti) adhesion layer were patterned on Si substrates with 290 nm of thermal oxide using electron beam lithography followed electron beam deposition and lift-off. Next, Ultra-thin and ultra-smooth TaS_2 flakes were produced by mechanical exfoliation from commercial available 1T TaS_2 crystals on Poly-dimethylsiloxane (PDMS) stamp and subsequently transferred on the top of the Pt electrodes[147] and heated to 300°C for 3 hours in ambient air to convert the its oxide form. Finally, top electrodes were fabricated by e-beam lithography and deposition of 10 nm Ti and 30 nm Au. The C-V measurements were done with an Agilent 4284A Precision LCR Meter with respect to the variation of bias voltage and frequency.

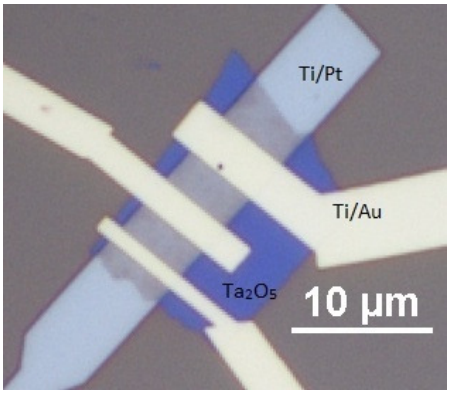

Fig. 7.2.1 MIM junction device of Ta_2O_5 dielectric for C-V measurement

7.2.2 FET DESIGN ELECTRICAL TRANSPORTMEASUREMENTS

Thin and ultra-smooth graphite flakes were made by mechanical cleavage method and transferred onto Si/SiO_2 substrates. Ultra-thin and ultra-smooth TaS_2 flakes were produced by mechanical exfoliation from commercial available TaS_2 crystals on PDMS stamp and subsequently transferred on the top of graphite by home built precision transfer stage. Optical microscope and Park-Systems XE-70 noncontact mode atomic force microscope were used to identify and characterize thin TaS_2 flakes. The substrates with thin TaS_2 flakes were heated at 300°C for 3 hrs in ambient environment to oxidize completely. The oxidized flakes were further characterized by optical microscope and XE-70 non-contact mode atomic force microscope. Few layer MoS_2 flakes were exfoliated on PDMS stamp and transferred onto oxidized TaS_2 flakes. Drain and source electrodes were defined on MoS_2 flakes by conventional e-beam lithography and gate electrode was connected to graphite. MoS_2 FETs were fabricated by electron beam deposition of 5 nm of Ti covered by 40 nm of Au. For top gate measurement, oxidized TaS_2 flakes on Si/SiO_2 substrate were pickup by using polycarbonate (PC) and transferred on the top of fabricated MoS_2 FETs. Top gate was defined on the top of transferred oxidized TaS_2 by e-beam lithography and subsequent electron beam deposition of 10 nm of Ti covered by 40 nm of Au. Transport properties of the fabricated MoS_2 FET devices were measured by a Keithley 4200-

SCS semiconductor parameter analyzer in a Lakeshore TTPX Cryogenic probe station under high vacuum ($1x10^{-6}$Torr).

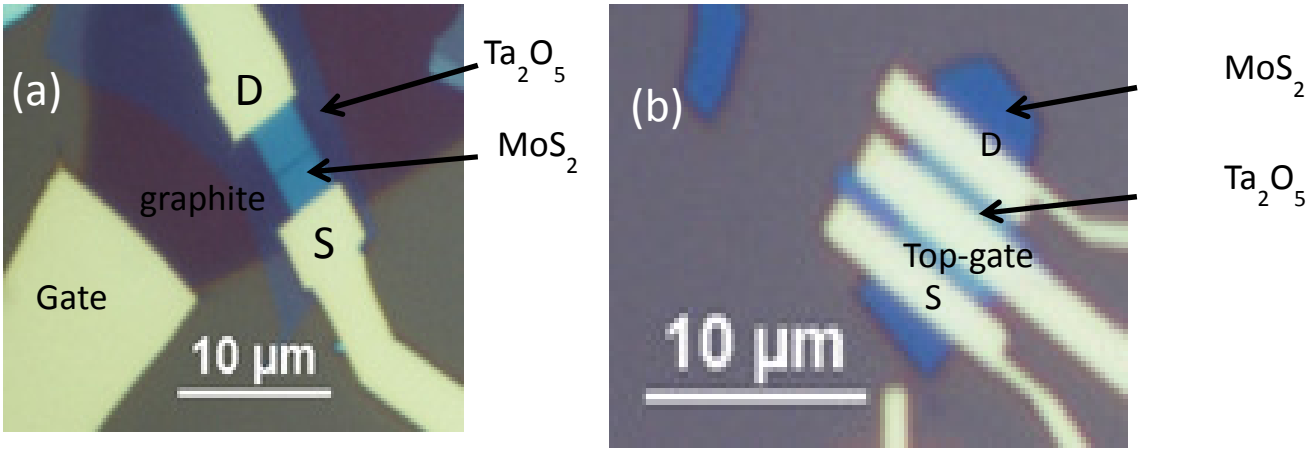

Fig. 7.2.2 optical images of MoS_2 FET devices (a) back gate configuration and (b) top gate configuration

7.3 RESULTS AND DISCUSSION

7.3.1 THERMAL ASSIST SYNTHESIS AND CHARACTERIZATION OF Ta_2O_5 FLAKES

First of all, TaS_2 flakes are prepared on Si/SiO_2 substrate by mechanical cleavage method and kept it on hot plate at 300°C about 3 hours in ambient condition. The optical contrast of the flakes under same field of view of optical microscope shows clear difference before and after thermal treatment as shown in **Fig.7.2.1 (a, b)** which might indicate different chemical composition. Then we characterized the surface topography of the flakes by non-contact mode AFM. The AFM image reveals that the surface features preserve after heating of TaS_2. **Fig.7.2.1 (c, d)** show the AFM images of TaS_2 flakes on Si/SiO_2 substrates before and after heating at 300°C for 3 hrs.

To reveal the surface chemical composition and chemical states before and after the heating, X-ray photoelectron spectroscopy (XPS)were performed by using a Kratos Axis Ultra XPS system with a monochromatic Aluminum (Al) source. The samples were exfoliated from

crystals right before XPS measurement and then immediately put into the XPS chamber to avoid oxidation since TaS_2 is sensitive to air. Pass energy of 20 eV were used with 0.1 eV scanning step for photoelectron detection. Carbon 1s reference line, 284.6 eV, was used to calibrate the charging effect. **Fig.7.2.1** (e, f) show Ta $4f_{7/2}$and $4f_{5/2}$ spectra before (red line) and after (black line) the oxidation. As can be seen in **Fig.7.2.1** (e, f), the Ta 4f orbit of transferred TaS_2 flakes has two peaks located at 22.7 and 24.7 eV, which are assigned to the doublet of Ta $4f_{7/2}$and Ta $4f_{5/2}$. It is clearly evident that after oxidation binding energies for $4f_{7/2}$andTa $4f_{5/2}$are shifted to 25.8 eV and 27.7 eV, consistent with the spectral profile of Ta_2O_5.[148-151] From the XPS spectra, it is evident that the process has successfully converted 2D TaS_2 into Ta_2O_5.

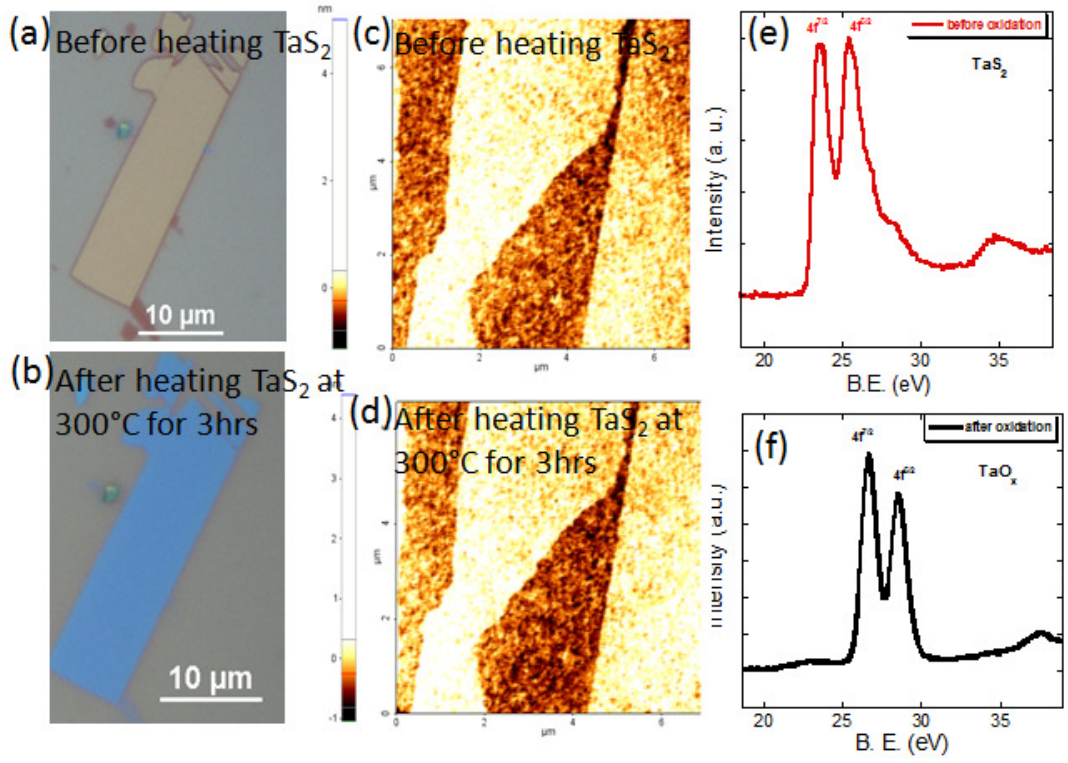

Fig.7.3.1 (a, b) Optical image of thin TaS_2 template on Si/SiO_2 substrate after transfer form scotch tape with repeated splitting of bulk 1T TaS_2 and corresponding optical image of template after heating at 300°C for 3hrs in ambient environment. (c, d) AFM image of TaS_2 template before heating and after heating at 300°C for 3hrs in ambient environment (e, f) XPS spectra of TaS_2 and synthesized Ta_2O_5

7.3.2 C-V MEASUREMENT

To find out the dielectric constant of as prepared dielectric from oxidation process, MIM junction is prepared by sandwiching oxidized TaS_2 in between two metal electrodes. Capacitance was measures by sweeping DC bias voltage with ac voltage keeping 100mV at frequency 500 Hz and 1 kHz. At both frequencies, we observed applied voltage is independent of value of measured capacitance. To test the consistency, we did C-V measurement for different thickness sample ranging from 5 nm to 35 nm and with multiple electrodes having different areas. The mean capacitance measured for given thickness varies linearly with area of electrodes and nearly passing through the origin. The linear dependence of capacitance with area suggesting the TaS_2 layers is completely oxidized irrespective of the thickness of the sample. The C-A curve passes through the origin suggests the negligible background/parasitic capacitance. **Fig.7.3.2** (a) inset shows the typical MIM junction device. It consists of 3 sets of MIM junction devices with different width of top electrodes and width of common bottom electrode is 5 μm. We can make seven MIM junction devices out of 3 electrodes by taking individual electrodes and possible distinct combinations of the electrodes in regards of their area for C-V measurements.

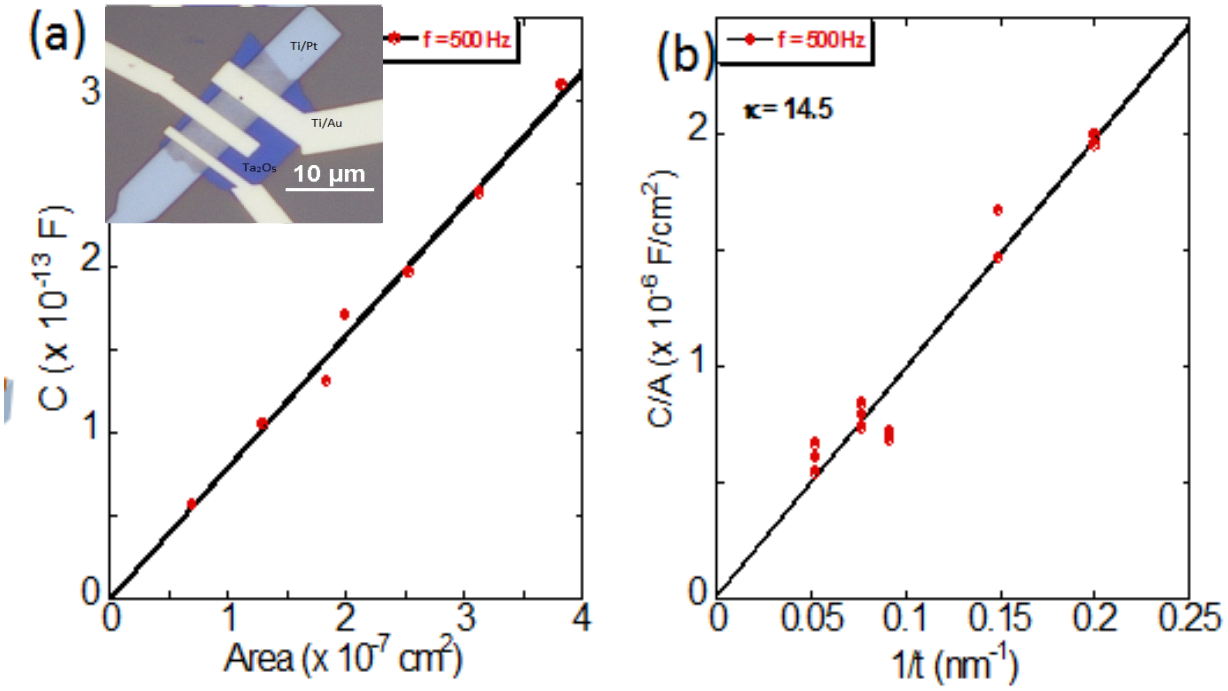

Fig.7.3.2 (a) Area dependence capacitance plot of 19 nm Ta_2O_5 dielectric measured by C-V measurement. Inset shows the optical image of corresponding device for C-V measurement. (b) Capacitance per unit area *versus* inverse of thickness of Ta_2O_5 plot. The slope of the plot gives the dielectric constant of Ta_2O_5 according to parallel plate capacitor model.

We extracted capacitance per unit area (C/A) of different thickness samples by measuring capacitance of corresponding Ta_2O_5 MIM devices. **Fig.7.3.2** (b) is the plot of capacitance per unit area with respect to inverse of thickness. The plot fits well with parallel plate capacitor model:

$$C = \frac{\kappa \epsilon_0 A}{t}$$

where C is capacitance, t is thickness, and κ is dielectric constant of Ta_2O_5, A is area electrode covering the Ta_2O_5 and ϵ_0 is permittivity of free space.

The linear relation C/A vs inverse thickness suggests the complete oxidation of TaS_2 by thermal oxidation approach. The dielectric constant is determined by using parallel plate

capacitor model. The dielectric constant (κ) of as prepared Ta_2O_5 is determined to be ~ 14.5 by capacitance-voltage (C-V) measurement.

7.3.3 TRANSPORT MEASUREMENTS IN BACK GATE CONFIGURATION

Electrical transport properties of the fabricated MoS_2 FET devices were measured by a Keithley 4200 semiconductor parameter analyzer in a Lakeshore Cryogenic probe station under high vacuum (~$1x10^{-6}$ torr). **Fig.7.3.3** (a) shows typical output characteristics (I_{ds} - V_{ds}) for a 3.9 nm thick MoS_2 device on 8 nm Ta_2O_5 measured at room temperature in back gate configuration. The I_{ds} - V_{ds} curves are linear at lower drain source voltage region and shows clear current saturation at sufficiently higher drain source voltage region. The observed current saturation is mainly caused by the reduction of the effective gate voltage and drain-source bias voltage due to the relatively metal-MoS_2 contact resistance. [152] The saturation current still has room to improve since we used metal electrodes which has non-negligible contact resistance. Contact phase engineering, using tunable electrode are the possible solution to further improve the device performance.[29, 107]

Fig.7.3.3 (b) shows the transfer characteristics of the same MoS_2 FET with drain source voltage (V_{ds}) is 100mV. We observed the n-type conduction with ON/OFF ratio is in the order of 10^5 and nearly hysteresis free transfer curve with ideal subthresold swing (SS) 64 mV/dec. This indicates that the Ta_2O_5 surface is charge impurities/traps, defects free surface and clean dielectric/channel interface. The long range Coulomb scattering originating from the charged impurities in the SiO_2 substrate or at the substrate/graphite interface are adequate to screen by graphite layers.[55, 153] In addition, the surface roughness of the Ta_2O_5 surface is comparable to mechanically exfoliated 2D materials like h-BN which reduces the surface roughness scattering of charge carriers on the MoS_2 channel.[154] Moreover, we don't observe the gate leakage current

for enough range of applied gate voltage. These properties of high-κ Ta_2O_5 dielectric are ideal for TMDs base FETs. The room temperature two-terminal field-effect mobility is calculated using the expression,

$$\mu_{FE} = \frac{L}{W} \times \frac{dI_{ds}}{dV_{bg}} \times \frac{1}{C_{bg}} \times \frac{1}{V_{ds}}$$

where L, W, V_{ds}, I_{ds} and V_{bg} are channel length, channel width, drain voltage, drain current, and back-gate voltage, respectively. C_{bg} is the capacitance per unit area of gate dielectric. The calculated two-terminal field-effect mobility of MoS_2 FET devices lies between 20-50 $cm^2V^{-1}s^{-1}$.

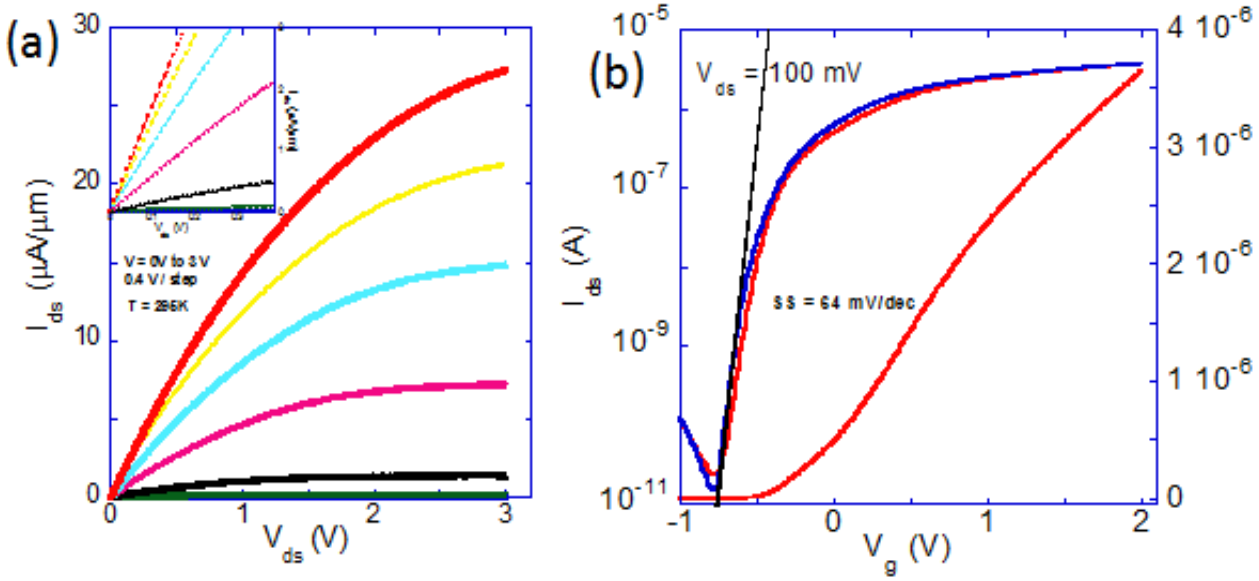

Fig.7.3.3 (a) Room-temperature output characteristics of the 6.0 nm MoS_2 device. Inset shows the linear I-V at low bias region. (b) Room-temperature transfer characteristics of MoS_2 FET device in semi-log and linear scale. Red color represents the forward sweep direction and the blue color represents backward sweep direction.

7.3.4 TRANSPORT MEASUREMENTS IN DUAL GATE CONFIGURATION

We also fabricated dual gate MoS_2 FET devices to characterize its transport properties. We measured the dual gated MoS_2 FET devices in single gate and dual gate configurations. We applied back gate voltage to tune the contact and the top gate to tune the channel region.

Fig.7.3.4 (a) shows the I-V characteristics of the 5.6 nm MoS_2 device in dual gate configuration with V_{bg} = 60 V with different top gate voltage from -2 V to 1V with 0.4 V step size. We observed clear the gate modulation and current saturation of output curve mainly caused by the reduction of the effective gate voltage and drain-source bias voltage due to the relatively metal-MoS_2 contact resistance. At low drain source voltage region as shown in **Fig.7.3.4** (a) inset, the current varies linearly with voltage and, at high drain source voltage region, drain source shows current saturation. We observed similar property for all back gate voltages ranging from 0V to 60V. **Fig.7.3.4** (b) and (c) depict the transfer characteristics of dual gate MoS_2 FET device in semi-log scale and linear scale at V_{ds} =100 mV. We calculated subthresold swing (SS) 61 mV/dec which is nearly same for all applied back gate voltages. We consistently observed similar values for all dual gated MoS_2devices. We calculated the mobility of the dual gated devices varies between 50-80 $cm^2V^{-1}s^{-1}$. The high performance and better electrical control is sensing for dual gated devices since the top gate is used to change the carrier density in the channel and back gate is effective to reduce the contact resistance.

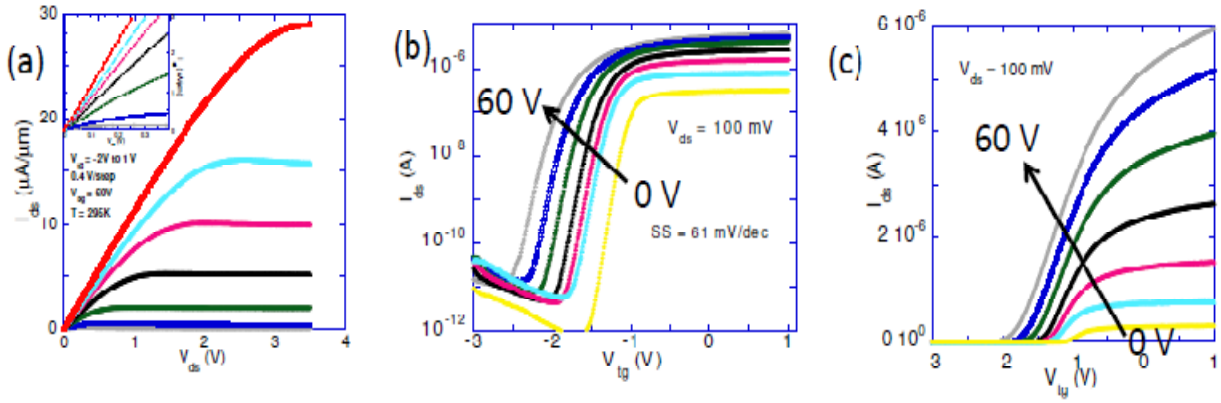

Fig.7.3.4 (a) Room-temperature output characteristics of the 6.5 nm MoS_2 device. Inset shows the linear I-V at low bias region. (b, c) Room-temperature transfer characteristics of MoS_2 FET device in semi-log and linear scale with different back voltages.

7.4 SUMMARY

In conclusion, we successfully developed the facile transformation of two dimensional transitional metals into high-κ dielectric transitional metal oxides. Optical contrast of thermally treated sample in oxygen environment shows clear color contrast, indicating the change of chemical composition during process. XPS measurements conforms the oxidation and C-V measurements determines dielectric constant. We fabricated the MoS_2 field effect transistors in back gate and dual gate configurations by using as prepared high-k dielectric. We demonstrated that the few-layer MoS_2 FETs fabricated on thermal-oxidation grown ultra-thin, atomically flat Ta_2O_5 flakes as bottom and top-gate dielectrics show high field-effect mobility, near ideal subthreshold swing, reduced hysteresis, and a high ON/OFF ratio at room temperature. We attribute improved performance of MoS_2 FETs on high quality tantalum oxide high-κ dielectric.

FUTURE WORK

We found that the dielectric environment is very important for the transport properties of TMDs based FETs. In addition, the contact material to study the intrinsic transport properties of TMDs channel is crucial. The fabrication process and strategy is equally important to make cleaner channel, interfaces between dielectric/channel and channel/contact surfaces.

We introduced a new facile approach to make amorphous transitional metal oxide (TMO) as potential candidates for high-quality high-κ dielectric for TMDs based field effect transistor and characterized transport properties in top and back gate configuration. The materials characterization of such prepared TMOs itself is the important path to test the quality of the materials and optimize the process to get better quality. In addition, working on the optimization of our thermal oxidation process to get high quality TMOs from layered materials is important task to establish universal method.

We found the as prepared TMO high-k dielectric has superior quality in terms of surface quality and surface defects states. Our transport measurements revealed reduced hysteresis, high two-terminal field-effect mobility, well saturated drain source current and low subthreshold swing (61 mV/dec) of MoS_2 FETs at room temperature. On the other hand, we characterized the two terminal pristine TMDs channel field effect by using p-doped/n-doped TMDs contact by van der Waals stacking method. The contact resistance of such contacts is as low as 0.3 kΩ μm, with high on/off ratios (up to $> 10^9$), high drive currents (exceeding 320 $\mu A\ \mu m^{-1}$) and record high cryogenic field effect mobilities (exceeding $2\times10^3\ cm^2\ V^{-1}\ s^{-1}$ at 5K). Our next step is to combine as prepared high-κ dielectric to 2D/2D van der Waals assembly to investigate to TMDs true channel properties. The integration of dielectric engineering and contact engineering is the exciting idea to investigate the true channel properties of TMDs field effect transistor. The

heterostructure of high κ dielectric and 2D/2Dvan der Waals assembly expected to reveal the true intrinsic limit of their electrical performance at low resistance ohmic contact.

Scaling is important for practical application of field effect transistor. But, as the channel length decreases, short channel effects come in to play and compromise the device performance. Top-gate n-type high performance TMDs FET has been readily achieved. However, high performance top gated p-type TMD devices, with high driving current, enough on/off ratio and sharp subthreshold swing, are also needed for high performance, low power complimentary electronics. The performance of p-type TMDs FETs is still largely limited by non-ideal contacts due to the presence of significance schottky barrier and non-ideal dielectric environment. Charge carriers are concentrated on the top surface of the channel in top gate configuration and separate from the bad gate dielectric which mitigates the back gate dielectric effect on the carriers of the TMDs channel materials. The integration of low resistance TMDs field effect transistor and as prepared TMOs high-k dielectric with optimize its thickness for the better control over the field effect transistor in low operating voltage is the ultimate idea to explore its true channel properties without short channel effect.

We developed unique method for low-resistance ohmic contacts achieved using the novel 2D/2D contact strategy and novel technique for dielectric integration. The next step is to explore the rich quantum physics in TMDs 2DEGs and 2DHGs by using the developed contact engineering and dielectric integration. It is expected to extract important information about the electronic structure of these systems, such as cyclotron mass, quantum scattering time, and degeneracy level and quantum phenomena such as quantum Hall effects.

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ABSTRACT

SUBSTRATE EFFECTS AND DIELECTRIC INTEGRATION IN 2D ELECTRONICS

by

BHIM PRASAD CHAMLAGAIN

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Advisor: Dr. Zhixian Zhou

Major: Physics

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The ultrathin body of monolayer (and few-layer) two dimensional (2D) semiconducting materials such as transitional metal dichalconiges (TMDs), black phosphorous (BP) has demonstrated tremendous beneficial physical, transport, and optical properties for a wide range of applications. Because of their ultrathin bodies, the properties of 2D materials are highly sensitive to environmental effects. Particularly, the performance of 2D semiconductor electronic devices is strongly dependent on the substrate/dielectric properties, extrinsic impurities and absorbates. In this work, we systematically studied the transport properties of mechanically exfoliated few layer TMD field-effect transistors (FETs) consistently fabricated on various substrates including SiO_2,Parylene –C, Al_2O_3, SiO_2 modified by octadecyltrimethoxysilane (OTMS) self-assembled monolayer (SAMs), and hexagonal boron nitride (h-BN). We performed variable temperature transport measurements to understand the effects of various scattering mechanisms such as remote surface phonon scattering, coulomb scattering, surface roughness scattering on the mobility of these devices. To reveal the intrinsic channel properties, we also investigated TMD devices encapsulated by h-BN. To further optimize the dielectric interface and electrostatic control of the TMD channels, we developed a novel thermal-oxidation method to

turn few-layer 2D metals into ultrathin and atomically flat high –κ dielectrics. In order to optimize the performance of TMD electronic devices, it is also critical to fabricate low resistance ohmic contacts required for effectively injecting charge carriers into the TMD channel. Along this direction, we developed a new contact strategy to minimize the contact resistance for a variety of TMDs by van der Waals assembly of doped TMDs as contacts and undoped TMDs as channel materials. The developed unique method for low-resistance ohmic contacts achieved using the novel 2D/2D contact strategy and novel technique for high-k dielectric integration is expected to open the path to explore the rich quantum physics in TMDs 2DEGs and 2DHGs.

AUTOBIOGRAPHICAL STATEMENT

BHIM PRASAD CHAMLAGAIN

EDUCATION

Ph. D.(Physics): Wayne State University, Detroit, Michigan, USA, 2011 - 2016
M. S.(Physics): Wayne State University, Detroit, Michigan, USA, 2011 - 2013
M. Sc.(Physics): Tribhuvan University Kathmandu, Nepal, 2003 - 2005
B. Sc.(Physics): Tribhuvan University Biratnagar, Nepal, 2001 – 2003

PROFESSIONAL EXPERIENCE

2011-2016: Graduate Teaching Assistant/ Graduate Research Assistant
Department of Physics & Astronomy, Wayne State University, Detroit, MI, USA
2010-2011: Physics Lecturer and Moderator of Science & Technology Club
St. Xavier College Maitighar, Kathmandu, Nepal
2010-2011: Physics Lecturer
Jubilant College Kalimati, Kathmandu, Nepal
2008-2009: Physics Lecturer
Nepal Police (the then Dipendra Police) Higher Secondary Barding School Sanga, Kavre, Nepal
2007-2008: Physics Lecturer
Tulsi Higher Secondary Barding School Tulsipur, Dang, Nepal
2006-2007: Science Teacher
Shree Little Buddhas' Academy Dallu, Kathmandu, Nepal

FELLOWSHIPS AND AWARDS

1. American Association of Physics Teachers (AAPT) Graduate Teaching Assistant Award (2016)
2. George B. & Eveline R. Beard Endowed student prize (2015)
3. Thomas C. Rumble Fellowships (2014 - 2015)
4. Dissertation Scholarship, Tribhuvan University (2005)
5. Outstanding Student Scholarship, Tribhuvan University (2001, 2002, 2004)

PUBLICATIONS/PRESENTATIONS

- Eight peer review publications including 3 *ACS Nano*, 2 *Nano Letter*, 1 *Advanced Materials*, 2 *Nanoscale* and 3 papers are in preparation
- Oral presentation in APS march meeting (2013, 2014, 2015, 2016) & Colloquium presentation in condensed matter & bio-physics colloquium, Wayne State University (2015)
- Poster presentation in Graduate Research Day, Wayne State University (2013, 2014, 2015, 2016), Nano Multidisciplinary Incubator Program Symposium and OSAPS conference 2012

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