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Two-Dimensional Low-Resistance Contacts For High Performance Wse2 And Mos2 Transistors

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TWO-DIMENSIONAL LOW-RESISTANCE CONTACTS FOR HIGH PERFORMANCE WSe_2 and MoS_2 TRANSISTORS

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CHAPTER 1 BACKGROUND AND MOTIVATION

Graphene, a single layer of carbon atoms packed into a 2D honeycomb lattice, was first successfully isolated by Novoselov et al. using a micromechanical cleavage method.[3] Since then it has quickly emerged as an important material for both fundamental research[4,5] and device applications in many areas, including electronics,[6,7] spintronics,[8,9] chemical, biological sensing,[10-13] nanoelectromechanical systems (NEMS)[14] and energy storage.[15] The band structure of graphene consists of conduction and valence bands touching each other at the charge neutrality level, leading to a zero band gap. Although the high carrier mobility and planar structure make graphene a promising candidate for many electronic applications, the zero band-gap poses a major problem for mainstream logic applications.[5,16] To overcome this bottleneck, many theoretical and experimental studies have focused on engineering an energy gap in graphene.[6, 17-22] A tunable band gap up to 250 meV can be induced by a perpendicular electric field in bilayer graphene.[23] A band gap can also be generated by strain[24] or graphene chemistry[25] or quantum mechanical confinement.[20,26,27] However, above methods either severely degrade the carrier mobility or requires a prohibitively large voltage. Alternatively, a number of layered transition metal dichalcogenides (TMDs) such as MoS_2, $MoSe_2$ and WSe_2 have not only demonstrated many of the "graphene like" properties that are desirable for electronics applications such as mechanical flexibility, chemical and thermal stability and the absence of dangling bonds, but also have a substantial band gap. For instance, single-layer MoS_2 has a direct bandgap of ~1.8 eV, which makes it a suitable channel material for low power digital electronics. Similar to graphene, atomic layers of covalently bonded S-Mo-S unites can be extracted from bulk MoS_2 crystals by a mechanical cleavage technique due to relatively weak van der Waals (vdW) interactions between the layers.

Nevertheless the carrier mobility in monolayer and few-layer MoS_2 FETs fabricated on Si/SiO_2 substrates was found to be typically in the range of 0.1 -10 $cm^2V^{-1}S^{-1}$, which is not only orders of magnitude lower than graphene but also substantially lower than the phonon-scattering-limited mobility in bulk MoS_2 (which is on the order of 100 $cm^2V^{-1}S^{-1}$ at room temperature.)[28-32] Radisavljevic et al. have reported that the mobility of monolayer MoS_2 FETs can be improved by depositing a thin layer of HfO_2 high-κ gate dielectric on top of MoS_2 devices, where the significant mobility enhancement was attributed to the suppression of Coulomb scattering due to the high-κ environment and modification of phonon dispersion.[33] In addition, MoS_2 FETs have exhibited very high on/off current ratio of ~10^8, good subthreshold swing (74 mV/decade), and good mechanical flexibility, opening up the possibility of high-performance and low-power flexible electronics [33-35].

In addition to conventional FETs, MoS_2 can also be used in various other applications such as energy harvesting[36,37] and optoelectronics.[38,39] However, it is not clear to what extent the observed mobility increase can be attributed to the screening of charged impurities and phonon dispersion modification. On the one hand, a temperature-dependent electrical transport study of monolayer and few-layer MoS_2 FETs by Ghatak et al. suggests that the relatively low mobility in MoS_2 FETs on Si/SiO_2 substrate is a channel effect, largely limited by the charged-impurity-induced electron localization.[34] On the other hand, Lee et al. showed that the mobility in MoS_2 FETs on Si/SiO_2 substrate can be largely underestimated due to the SB at the MoS_2/metal contacts.[40] A result shows that mobility increase in polymer electrolyte covered monolayer MoS_2 FETs can be attributed partially to the reduction of contact resistance and partially to enhancement of the channel mobility.[41] As one of the most studied member of the TMD family, MoS_2 has emerged as a promising channel material for field-effect transistors with relatively

high on/off ratio and reasonable electron mobility. With the recent observation of indirect to direct bandgap transition, MoS_2 based optoelectronic devices has also attracted interest from the optoelectronics society.[147-156] In addition, due to the atomically-thin, flexible, and biocompatible nature of TMDs, a completely new generation of electronic sensor devices can be envisioned.[157-163] Furthermore, TMDs are desired candidate materials for thin film transistors[164-167] due to their excellent mechanical flexibility and optical transparency as well as for sensor and detector applications due to their high surface to volume ratio. Finally, TMDs can be used for energy harvesting due to their extraordinary light absorption capability and current conversion efficiency.[168]

1.1 Challenges in 2D electronics

The strength of semiconducting 2D TMDs (i.e. MoS_2, $MoSe_2$ and WSe_2) as channel materials lies in their sizable bandgap which varies according to the thickness of TMDs. For example, multilayer MoS_2 has an indirect bandgap of 1.2 eV, bilayer MoS_2 has indirect bandgap of 1.3eV, and single layer MoS_2 has direct bandgap of 1.8 eV. Also note that Bulk MoS_2 as a n-type semiconductor has an electron affinity of ~ 4 eV, and that of atomically thin MoS_2 is expected to be even smaller due to the increased band gap.[40, 43] This sizable band gap of TMDs results into a very high on/off current ratio and excellent electrostatic integrity.[147] However, TMD electronic devices often fail to form good (ohmic) contacts due to the work function mismatch between TMDs and most commonly used metals. This work function mismatch along with fermi-level pinning often results in a significant SB at the interface between TMDs and metal contacts. When a few layer MoS_2 is in contact with Ti (work function is 4.33eV,) electron injection from contact to channel(n-type) of the device can be easily formed whereas the hole injection from contact to channel is inhibited due to the significant SB formed at the contact

region. Moreover, the ambipolar behavior with relatively small current for both electrons and holes (shows in Fig. 3.4(a)) is observed from transport measurement of multilayer WSe_2 FETs, suggesting that the fermi level of few layer WSe_2 is close to the meddle of the band gap. As a result, a significant SB (more than 200meV for both electrons and holes) is formed for both the electron and hole channels with Ti as a contact metal.

In Fig. 1.1, a work function mismatch is present when the TMDs are in contact with many of the most commonly used metals, where a SB is formed at the contact interface. As shown in Fig. 1.1(a) and (b), the barrier between MoS_2 and metal for the electron channel is significantly smaller than the case of WSe_2, yet a large barrier tends to form for the hole channel in both cases. Large bandgap semiconductors are known to have difficulties forming ohmic contacts with metal, while low resistance ohmic contacts are essential in optimizing the device performance of FETs. There are typically two types of low resistance ohmic contacts that can be made between a semiconductor and a metal: (a) very low barrier Schottky contacts and (b) tunneling contacts with extremely thin barriers. Ideally, an ohmic contact can be formed if the SB height is zero or negative. For an n-type semiconductor such as MoS_2, the work function of the metal must be close to or smaller than the electron affinity of the semiconductor in order to form ohmic contacts. However, the work function of most commonly used electrode metals range from slightly over 4 eV for Al and Ti, over 5 eV for Pd and Ni. In addition, a good electrical contact material also requires high conductivity, chemical, thermal, electrical stability.

Unfortunately, it is extremely difficult to find metals with both stable electrical properties and low work function. Low-work-function metals such as Ca (which has a work function of 2.9 eV) can be oxidized easily leading to severely degradation of electrical characteristics. Therefore, it is challenging to find a suitable metal to form very low barrier Schottky contacts to n-type

TMDs. As for p-type semiconductors, the work function of the metal must be close to or larger than the sum of the electron affinity and the band gap, which is similarly challenging. Although relatively good contacts have been reported in monolayer WSe_2 FETs with high work function metal contacts, a non-negligible SB still appears to be present.[44] Furthermore, the Schottky barrier in the reported MoS_2 FET devices with various metal contacts appears to be quite insensitive to the work-function of contact metals, suggesting that the presence of Fermi level pinning is likely due to the metal induced gap states at the metal to MoS_2 interface.[45]

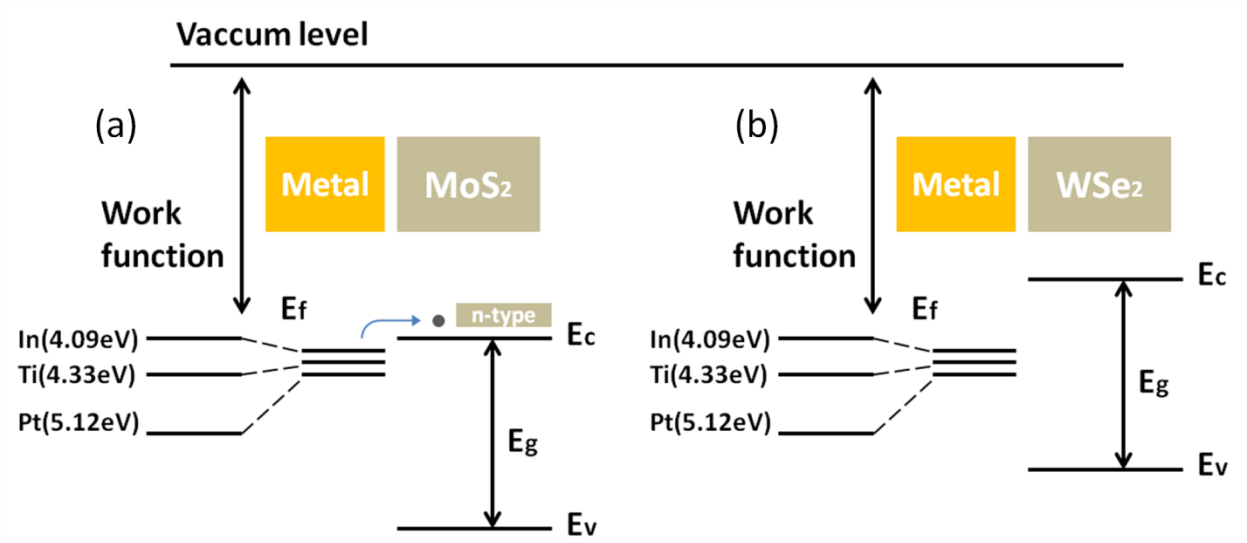


Figure 1.1 Fermi level pining due to the work function mismatch between metal and (a) MoS_2 and (b) WSe_2, where three commonly used metal is presented along with its work function. (a) n-type can be achieved since the fermi level of metal is close to the conduction band edge. In the contrast, (b) significant barrier is presenting in WSe_2 to metal for both electron and holes.

An alternative is to make narrow Schottky junctions, where the contact resistance is determined by the tunneling current. In order to achieve low contact resistance in narrow Schottky junctions, the SB height must be small and the ionized impurity concentration in the semiconductor must be large.[46] But the 2D nature of strongly layered materials makes it difficult to realize ionized impurity doping without substantially degrading the structural integrity of the atomically thin channel.

Yu et al. have demonstrated that the work function of graphene can be tuned by electric field effect within the range of 4.5 -4.8 eV for single layer and 4.65-4.75 eV for bilayer graphene using a Si back gate with a 300 nm thick SiO_2 dielectric layer, making graphene an attractive material for low contact barrier electrodes[47].

1.2 Approaches to engineering low-resistance contacts in TMD devices

There are typically two approaches to achieve low-resistance contacts between a semiconductor and a metal: (a) lowering the SB height by selecting contact materials with an extremely high (for *p*-type semiconductors) or low (for *n*-type semiconductors) work function, and (b) thinning the barrier width by degenerately doping the contact regions.

1.2.1 First approach

In the first approach, high performance TMD FETs with low resistance contacts can be achieved[1] by using Graphene as a work-function-tunable electrode material for atomically thin layered TMDs. However, a large range of work function tunability will be needed for achieving true Ohmic contacts for both electrons and holes in graphene/TMD junctions due to the large band gap of the TMD materials. To resolve this issue, usage of the extremely large electric double layer (EDL) capacitance of an ionic liquid (IL) gate is introduced where it can effectively tune the carrier density (thus the work function) of graphene. An ionic liquid gate can induce a high carrier density exceeding 10^{14} cm^{-2} in graphene, which is more than an order of magnitude higher than using a conventional solid-state gate dielectric.[49]

As a result, we have formed for the first time, in a single device structure, WSe_2-based FETs of both n- and p-type that display low-resistance contacts (down to ~ 2 kΩ.μm) and a high carrier mobility (> 300 $cm^2V^{-1}s^{-1}$ at 77 K), which will be discussed in detail in Chapter 3. However, for realistic device applications, methods to achieve more permanent, air-stable and

thermally stable ohmic contacts with an order of magnitude lower contact-resistance are urgently needed.

1.2.2 Second approach

Various doping methods such as surface charge transfer doing[51-54] and substitutional doping[5-6] have also been developed by different groups during the past few years to reduce the SB width and thus reduce the contact resistance of TMD devices.

While most of these doping methods suffer from poor air or thermal or long-term stability, substitutional doping with dopants secured by covalent bonding (e.g. Nb doped MoS_2) offers excellent air and thermal stability needed for practical device applications[6]. However, substitutional doping achieved during synthesis is not practical for creating selectively doped drain and source regions with a spatially abrupt doping profile needed for low power, high performance electronics. FETs fabricated from Nb-doped MoS_2 have shown reduced gate tunability of the channel and mobility degradation due to charged impurity scattering[6]. Ideally, one would like to selectively dope the drain and source regions under metal electrodes while leaving the channel region un-doped. In silicon-based electronic devices, this is achieved by heavy ion implantation doping of the drain and source contact regions under the metal electrodes. As a result, the contact material in silicon devices is a degenerately doped and highly conducting version of the channel material, which forms i) a highly transparent contact with the top metal, and ii) a barrier-free contact with the channel (in the on-state). However, the 2D nature and atomic thickness of strongly layered materials such as TMDs prevents controlled heavy doping by ion implantation without substantially compromising the structural integrity of the atomically thin channel. On the other hand, the weak vdW like interlayer bonding in layered 2D materials such as TMDs opens up new opportunities for developing new materials and device architectures.

Along the direction of the second approach: 2D/2D contact strategy which thinning the barrier width by doping the regions under or at the edges of the contacts. Different 2D materials can be artificially stacked on top of each other to form heterostructures with atomically sharp interfaces, without the constrains of atomic commensurability, due to the lack of dangling bonds on their surfaces and their inherent mechanical flexibility. Atomically thin p-n junctions consisting of vertically stacked MoS_2 and WSe_2 layers have been recently demonstrated.[55-58] They are fundamentally different from conventional p-n junctions. Specifically, the built-in potential in 2D/2D p-n junctions is dropped across the vdW gap without an obvious depletion region, and thus charge transport across the atomically thin 2D/2D p-n junctions is dominated by quantum mechanical tunneling through the vdW gap. As a result, charge transfer across the atomically thin junctions is ultrafast, as evidenced by the recent experimental observations of strong photocurrents and quenching of photoluminescence signals in MoS_2/WSe_2 p-n junctions, which was further verified by transient absorption measurement.

In these aspects, we propose a new contact paradigm based on 2D/2D vertical junctions, by innovatively integrating heavily doped TMDs as drain/source contacts and their undoped counterparts as the channel materials through vertical vdW assembling. To achieve low resistance ohmic contacts, it is essential to eliminate the energy barrier at the 2D/2D interface that hinders the electron (hole) transport across the junction due to the conduction (valence) band offset ΔE_C (ΔE_V.)[57-59] The Device fabrication of the first and second approach will be addressed in greater detail in chapter 2, and results will be discussed in chapters 3 and 4.

CHAPTER 2 SAMPLE PREPARATIONS AND DEVICE FABRICATIONS

In this chapter, we introduce techniques that are needed to fabricate high performance TMDs FETs. From the fundamental mechanical exfoliation method of TMDs crystal to the core of the vdW assembling is discussed in great detail in this section. The Dry transfer methods we developed plays an important role in this project, covering both graphene contacted and doped-TMD contacted TMD devices.

2.1 Samples Preparation

2.1.1 Crystal synthesis

All our TMD crystals (WSe_2, $MoSe_2$, $NbWSe_2$, $ReWSe_2$, and $NbMoS_2$) were synthesized by chemical vapor transport using iodine as the transport agent except undoped MoS_2 crystals, which were purchased from SPI Supplies, Graphite crystals was purchased from SPI Supplies, and hBN crystals were purchased from 2D semiconductor supplies.

The as grown crystals were phase-pure as determined by x-ray diffraction. Atomically thin TMD flakes were produced from the bulk crystal by a mechanical cleavage method. And an optical microscope was used to identify thin flakes, which were further characterized by Park Systems atomic force microscopy (AFM) in the non-contact mode. In this project, high quality single crystals are provided by Dr. David Mandrus' group at the University of Tennessee[2].

All TMD crystals[1, 2] were synthesized by chemical vapor transport using iodine as transport agent. Single crystals of WSe_2 ($MoSe_2$) were grown as follows. Polycrystalline WSe_2 ($MoSe_2$) was first synthesized from a stoichiometric mixture of W (Mo) (Alfa-Aesar, 99.999%) and Se (Alfa-Aesar, 99.999%) powders. The mesh size is -22 for W (Mo) and -200 for Se. The starting materials were sealed in silica tubes under vacuum, and then slowly heated to 900 ^{o}C.

The ampoules remained at 900°C for seven days, and then furnace was cool to room temperature. Single crystals of WSe_2 ($MoSe_2$) were then grown using the polycrystals as starting material and iodine as a transport agent (~17.5 mg/cm^3 of iodine). The silica tubes containing phase-pure powder and iodine were sealed under vacuum and placed in a tube furnace with a 50°C temperature gradient from the hotter end of the tube containing the charge (1050°C) to the colder end where growth occurs (1000°C). The silica tubes with the powder inside were evacuated, backfilled with argon, then again evacuated, backfilled with argon, and evacuated one last time before sealing. Crystals in the form of shiny silver plates with typical size 5 × 5 × 0.1 mm^3 grew over the course of 5 days. The as-grown crystals were phase-pure as determined by x-ray diffraction.

For doped TMD crystals, 0.5% of Niobium (Rhenium) was used as substituent atoms for p-doping (n-doping), following similar procedure for growing undoped WSe_2 ($MoSe_2$) crystals. The only difference comes with the vapor transport. For the doped samples, the temperature gradient is from 1035°C to 985°C. In all cases, the heating rate was 1°C/minute, the samples dwelled about 5 days, and then furnace cooled. The purity and mesh of the dopants are as follows: Nb = -325 mesh, 99.99% pure, metals basis excluding Ta (Ta ≤ 500ppm); Re = -22 mesh, 99.999% pure.

2.1.2 Chemical Vapor Deposition (CVD) Growth of Single-layer Graphene

The CVD graphene was grown on the clean copper foil (Alfa Aesar) which has taken to the surface cleanness treatment in order to improve the surface smoothness of a copper foil which was treated in Acetic acid bath and followed with the DI water and Isopropyl Alcohol (IPA) rinse cleaning. Annealing process was then introduced after the copper foil cleaning process. It treated under the vacuum condition for 1 hour with 5 sccm flow rate of H_2 gas alone

with the pressure around 0.4 mTorr at 1000°C. After annealing, flow the H_2 gas with 3 sccm flow rate for the entire growing procedure. The growing condition temperature is controlled as the temperature increase from room temperature to 1000 °C in 100 minutes, then mixture gas of CH_2 (35 sccm and H_2 gas with 3 sccm) were flown into the furnace for graphene growth for 30 minutes. Cool down to the room temperature, the setup is showing in Fig. 2.1

Figure 2.1 (a) The MTI Corporation OTF 1200x (1200C Split Tube Furnace with Vacuum Flanges and Optional Quartz Tube 100 mm O.D.); (b) The clean copper foil (Alfa Aesar) after annealing; (c) The copper foil with CVD thermally growth monolayer graphene after cooling down.

The standard cleaning (RCA) and transfer procedure[60-62] is then introduced to extract the clean graphene sheet from copper foil after the grown procedure. First, cut the prepared graphene/copper foil into desired size (1cm by 1cm), then spin coated with the PMMA 950A2 (4000rpm in 40 seconds) then air dried. Second, 10 second oxygen plasma was then introduced to etch out the back-side of PMMA/graphene/copper foil.

Next, immersing the PMMA/graphene/copper foil into the copper etchant (1 mole of $FeCl_3$) for 3 hours or commercially purchased ammonium persulphate (APS) for 18 hours. After

this step, the thin film (PMMA /graphene) can be seen floating on the copper etchant. Finally the RCA clean procedure was introduced to clean the etchant residue during the etching process. The RCA cleaning procedure is introduced as following in Fig. 2.2 and Fig. 2.3. First, carefully scoop out the floating film (PMMA/graphene) on the copper etchant by a clean thin glass slide, transferring it into DI water, set for few minutes. Next scoop it from DI water and transfer into first solution of NH_4OH: H_2O_2: H_2O (20:1:1) for 15 minutes, then second solution HCl: H_2O_2: H_2O (20:1:1) for 15 minutes. Finally, finishing with transferring into DI water (notice that it is important to transfer in to clean DI water between each solutions). After RCA Clean, now we can use the prepared substrate to scoop out the graphene sheet with 10 minutes air dried and hot plate baking 10 minute from room temperature to 150 ^oC followed by the acetone bath to remove the PMMA layer. AFM then was used to characterize the surface cleanness and the roughness of the graphene.

Notice extra steps might be introduced to smooth the surface of the graphene in order to prevent the bubbles and wrinkles of the graphene after transferring. First, one drop of same PMMA (PMMA 950A2) which was used previously on the copper foil, and let it set for a few second to gently dissolve the dried PMMA layer in order to reduce the surface tension of the graphene sheet,[62] then 3000 rpm spin rate in 40second was applied, air dried for 10 minutes, 10 minutes acetone bath to remove the PMMA layer.

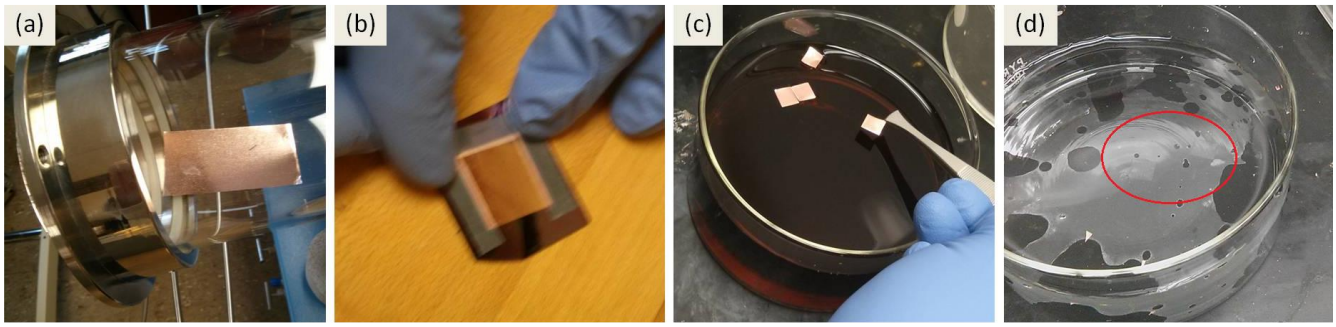


Figure 2.2 (a) The CVD graphene on the copper foil after growth; (b) Cut (a) intto smaller piece an tape to a holder in order to coat PMMA, then back side oxygen plasma etching; (c) Cut (b) into desired size(~1cmx1cm) and put into the cooper etchant where $FeCl_3$ as copper etchant; (d) transfer into the DI water following with the RCA clean procedure, notice the red circle indicates two pmma/graphene sheets floating on the DI water.

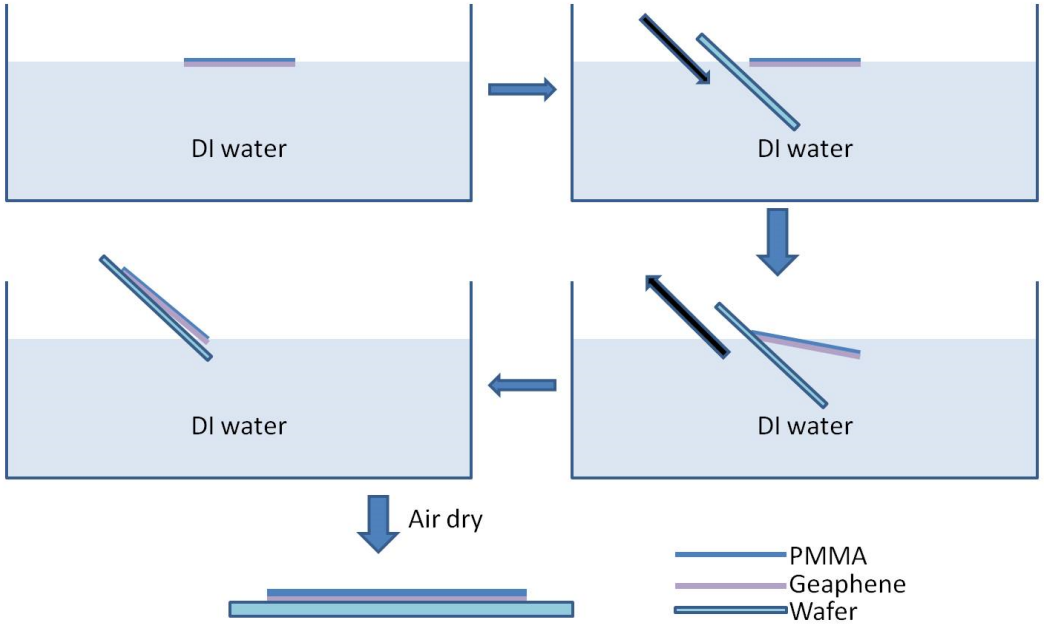
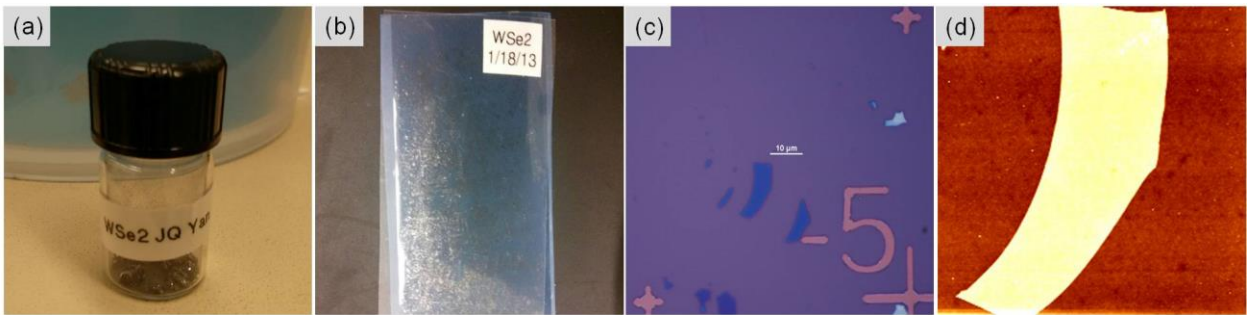


Figure 2.3 The simple flow chart shows the procedure of transferring after the copper etching process in Fig.2.2(d); To transfer the graphene/pmma, first immerse the clean glass slide or wafer, and slowly scoop out the graphene.

2.2 Preparation and characterization of ultrathin TMD crystals

In this project, we used the well-developed exfoliation method with the ultralow residue tape (Ultron system R1007 tape.) Ultrathin TMD crystal exfoliated on SiO_2/Si substrates were identified by optical microscopy and further characterized by Park Systems Atomic Force Microscopy (AFM) in non-contact mode as shown in Fig.2.4.



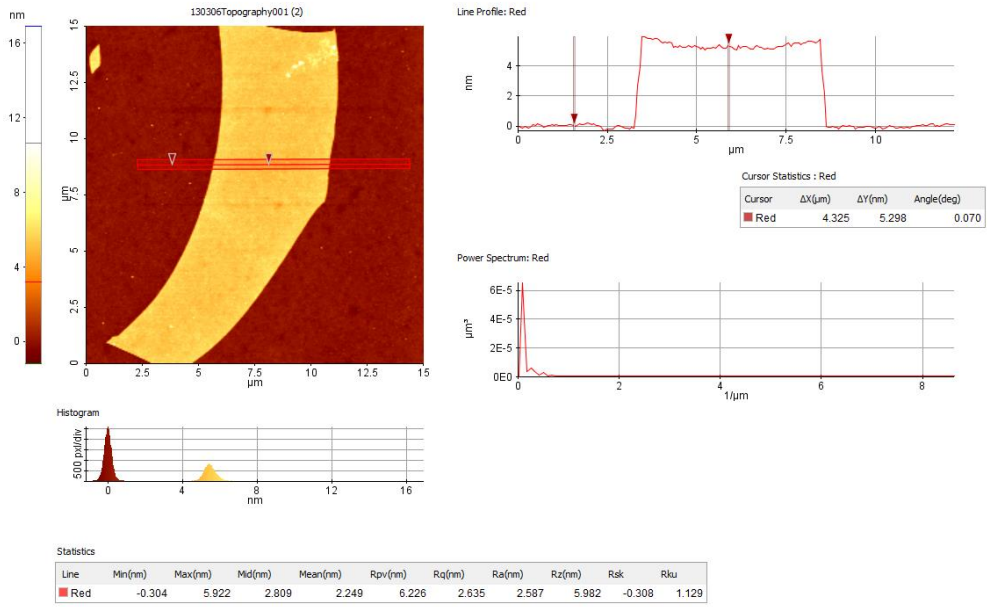


Figure 2.4 (a) High quality WSe_2 bulk sample; (b) Exfoliated WSe_2 flakes on ultra-low residue tape (blue tape); (c) The optical image of the WSe_2 samples on SiO_2/Si substrate, where the scale bar is 10 µm . (d) The AFM image of one of the WSe_2 samples in (c).

Before exfoliation, the clean Si Wafer with 290nm insulating layer (degenerately doped silicon substrate covered with a 290 nm-thick thermal oxide layer) substrate was prepared by the standard cleaning procedure. First, the as prepared substrates were bath sonicated in acetone and IPA bath for 15 minutes each. Then they were N_2 blow dry, followed with annealing in vacuum under 600^{o}C for 10 minutes along with flowing forming gas (10 % H_2/90%Ar) for two minutes upon reaching 600 ^{o}C. Second, gently press the prepared ultra-low residue tape (Fig. 2.4(b)) on the pre-cleaned wafer, the optical microscope was introduced to roughly determined the thickness of the target flakes followed with the atomic force microscope (AFM) to estimate the surface roughness, cleanness, and thickness of the flakes.

However, this conventional method is suitable for producing TMD FETs on SiO_2 substrate where the device performance can be suppressed by surface roughness of SiO_2. In order to overcome this issue, using a thin hBN flake (ultraclean and atomically smooth surface) as a

substrate is needed where the dry transfer techniques are introduced for device fabrication. This dry transfer techniques involve two type of methods, the Dry transfer method and the Pick-up-transfer method. Both methods will be well addressed in details in the following sections .

2.3 Dry Transfer method, and preparation

The Dry transfer method introduced in this section is one of the core techniques I developed in this project. Not only it allows us to achieve higher performance of devices, but also allows us to have access to other possibilities for high quality devices in many different applications.

2.3.1 PDMS stamp preparation

PDMS is one of key material that used for the dry transfer method. Freshly made PDMS stamps are crucial to producing vdW stacks of various 2D crystals with clean interfaces.

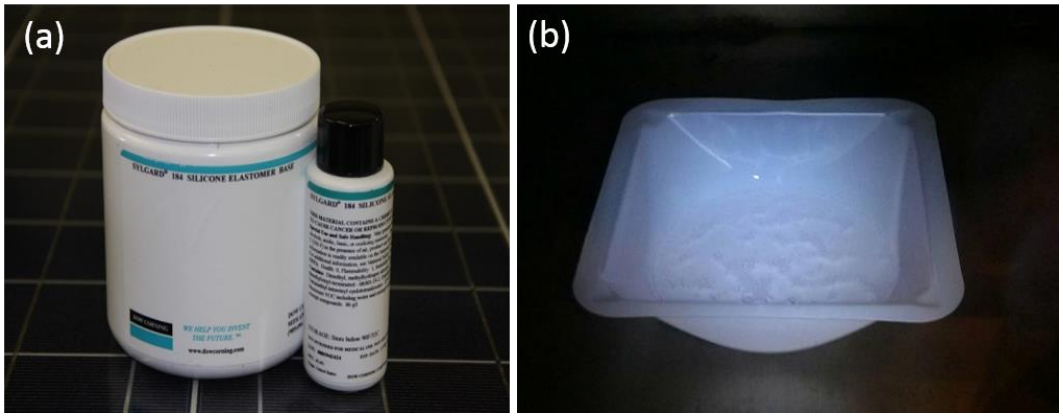


Figure 2.5 (a) The PDMS components, elastomer base (left in (a)), and curing agent (right in (a)), (b) Shows the PDMS mixture inside the vacuum chamber for de-bubbling purpose.

The PDMS patches were prepared from **SYLGARD 184 SILICONE ELASTOMER KIT** which contains two parts: Elastomer base, and curing agent (http://www.dowcorning.com) as shown in Fig. 2.5. First, gently and thoroughly mixed two parts with the weight ratio of 10: 1(e.g. 7g of elastomer base and 0.7g of curing agent.) Then the mixture is placed in a vacuum chamber for de-bubbling purpose for 20 minutes (Fig. 2.5(b)) followed with spin coating onto a

clean polished 4 inch silicon wafer at a spin rate of 350 rpm for 35sec. The thickness of PDMS is approximately 300-500um. Next, we placed the pre-coated PDMS wafer onto a hot plate preheated to 80^{o}C allowing it to cure for 30 minutes in air and another 30 minutes to cool down.[63] As the PDMS patch is prepared on the wafer, gently use acetone and IPA to clean the sharpened blade when cutting the PDMS into small pieces (1cm by 1cm.) for the ease of handling. Now it can be used for the generally dry transfer method or the pickup method which is discussed in the following section.

2.3.2 General Dry Transfer method

Since the PDMS is clean, clear and transparent, it can be used as a transfer stamp instead of using traditionally exfoliation method which is directly use the tape with TMD flakes on to the wafer substrate and gives lack of control to its position and selection to the target flakes. By using the PDMS patch along with homemade micromanipulator, the desired sample can be now be transferred on to the desired position and location.

The layered material flakes is first exfoliated onto blue tape from the single crystal as in Fig. 2.3(b)) following with placing the PDMS patches onto the prepared blue tape, then carefully remove (peel off) the PDMS stamp and place on to the edge of a clean glass slide with up-side down in which the thin flakes of TMD on the PDMS stamp is facing up. The desired thin flakes will be ready to transfer to the target location with the micromanipulator once it is found by the optical microscope.

First, place the base substrate (SiO_2/Si substrate as an example) on the sample holder under the optical microscope, then clamp the glass slide with TMD flakes/PDMS patch upside down on the homemade micromanipulator under the optical microscope where the thin flake can be seen clearly through optical microscope. First, focus on the base substrate and find the desire

location as the target location. Once the location is set, then focus back on the target flaks on PDMS patch, repeat this focusing steps until the target flakes and the target location is roughly aligned, Once it is ready, focus back to the base substrate, then gently lowing the glass slide/PDMS patch with the micromanipulator, adjust the in plane position if needed. While slowly lowering the glass slide, the contour of a target TMD flake should be gradually seen clearly. Note, it is still focused on the base substrate when lowering the glass slide/PDMS patch. Before overlapping the flake to the desired location, adjust the position from the micromanipulator and the orientation of the based substrate. Next gently approach to overlap the flakes to the location, the color different should be seen when PDMS patch touching the substrate. Lift up the glass slide, the flakes should be transferred on to the desired location on the base substrate. In Fig. 2.6, it shows the result of Fig. 2.6(1) to (2) as a one transfer, repeat the same procedure expressed above for other flakes to form the final device Fig. 2.6(4). The alignment procedure is addressed as following. As an example of Fig. 2.6(1) is our base substrate, we first adjust the x and y position (in plane position) of the flakes/PDMS/glass slide to align both target based substrate and flakes/PDMS/glass slide, then rotate the orientation of the Fig. 2.6(1) to nearly parallel to the TMD flake's orientation since the orientation of the TMD flake is harder to change, so that the TMD flake can be fully landed on the bottom h-BN flake as shown in Fig. 2.6(2.) Another example shows by rotating the orientation of Fig. 2.6(2), we can transfer the top hBN flake nearly perpendicular to the TMD flake to cover the its channel while leaving both end sticking out and gives us easy access to define the channel length as shown in Fig. 2.6(3.)

The step by step flow chart of procedure set up and transferring steps in order to transfer flakes on to desired position is showing in Fig. 2.7.

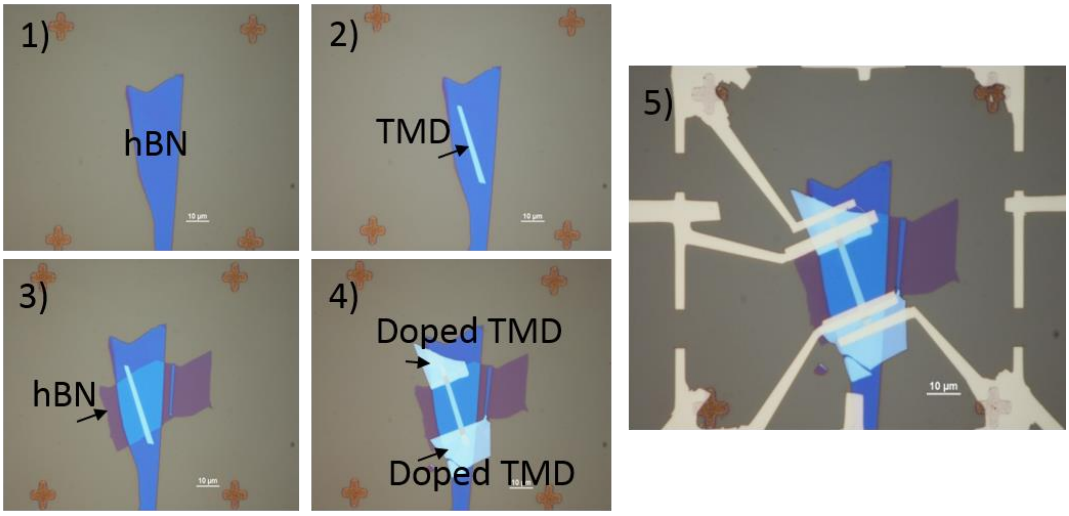


Figure 2.6 Shows step by step to form the vdW assembly stacking device following with the order from (1) to (4,) then finishing with the standard EBL follow by metal deposition. Notice from (1) to (2) indicates one complete transfer step expressed above, same for (2) to (3), and (3) to (4.)

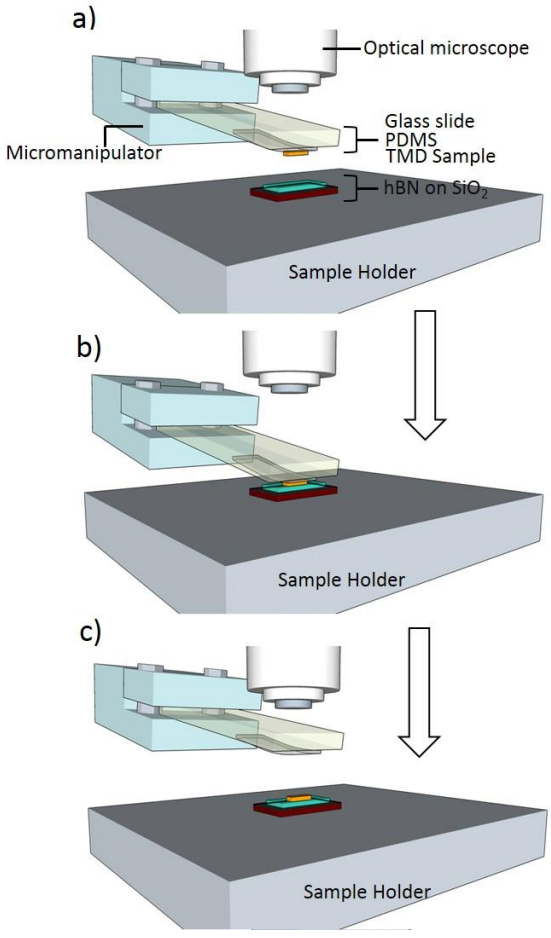


Figure 2.7 Schematic illustration of the process to transfer WSe_2 (yellow) onto hBN (blue) using a transfer stage equipped with a micromanipulator and a long working distance microscope objective. (a) Showing the preparation in which to align the WSe_2 to the desired location through the optical microscope (b) approaching by controlling the micromanipulator (c) lift off gently, the WSe_2 is now transferred on to hBN.

2.3.3 PC film preparation, and Pick-up transfer method

One of the other transferring method is to use Polycarbonate (PC) film to pick up the desired sample on the substrate and transferring it to the desired place. In our project, it is important to use to produce the transfer line method TMD devices to verify the contact resistant of the homo-junction device. The preparation of the PC is as following.

First, the Polycarbonate is dissolved completely and uniformly in chloroform with the weight percentage of 6%, then prepare desired sample on the pre-cleaned wafer substrate such as Fig. 2.4. Next, gently put a drop of PC solution (~0.018ml.) on the substrate and brush the surface with a clean piece of weighing paper to form a uniform thin PC film before it dries. Subsequently, put a small piece of pre-cut PDMS on top of the PC film in the sample area, gently scratch off PC film along the boundary of the PDMS piece using a clean razor blade, and peel off and clean up the rest of the area, so that only the patch of sample/ PC/PDMS remains on substrate and ready to be picked up. Next, use few drops of (~0.002ml.) clean deionized water to the edge of the patch. The patch should be released from the SiO_2 surface and floating on the DI water, carefully take the patch and flip upside down and place on to the clean glass slide, then quickly and gently blow try the DI water on the patch with N_2. It is now ready for transferring. The transfer step is same as in the previous section, yet the gentle heating to 135^{o}C will be introduced after touch down the PC film in order to release the PDMS from the PC film, then lift up the glass slide, air cool down to room temperature. Notice, the pc film could pop off while cooling down due to the surface tension and fast cooling, in this case, put it back to the preheated substrate holder to soften the pc film.

To remove the PC film, 5 minutes soaking in the 30ml of chloroform is used to dissolve the PC film from the base substrate for the initial cleaning, follows with another new 30ml of chloroform bath for 5minutes, repeat this procedure if needed. IPA raising, and N_2 blow dry after.

The flow chart of transferring steps (Fig. 2.8) for pickup thin flakes on to desired position is showing below.

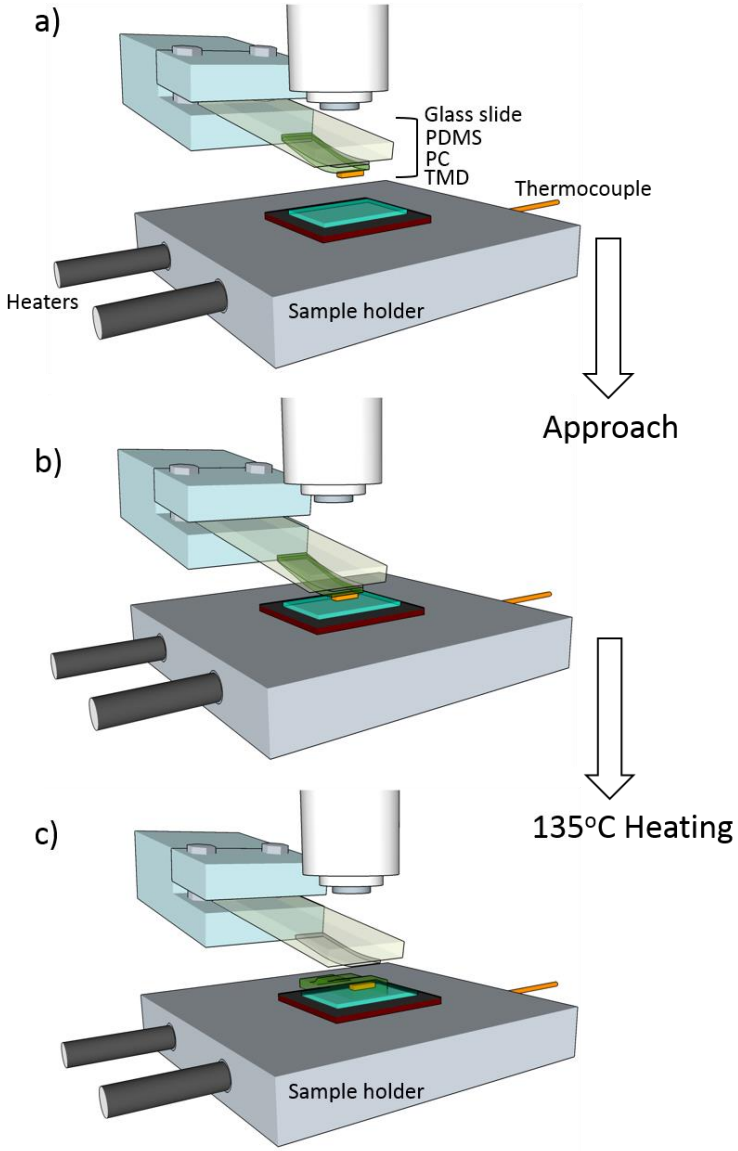


Figure 2.8 Schematic illustration of the process by using pick-up transfer method, from (a) the transfer patch contains PDMS/PC/TMDs was prepared and place onto the clean glass slide. Following with (b) the same procedure of regular dry transfer method showing in the previous section; (c) after approaching to the target sample or target position, heat up the sample holder

from room temperature to 135^{o}C, when reaches the temperature, hold for few minutes, then gently lift up the glass slide by the micromanipulator, the PC/TMD part should be separated from PDMS/glass slide easily. Air cool down to room temperature. Finally soak the substrate with transferred PC/TMD into chloroform, IPA rinsing and N_2 blow dry.

2.4. Device Fabrications

2.4.1 Graphene contact Sample preparation, device fabrication

In order to form the graphene contacted FETs device, first, thin h-BN crystals (10 - 50 nm thick) were first exfoliated from commercially available hBN crystals onto a PDMS stamp. Using a home-built precision transfer stage, they were subsequently transferred onto a few-layer WSe_2 flake to cover its middle section while exposing its two ends for electrical contacts. The graphene used in this study was grown on copper using a chemical vapor deposition (CVD) method.[64-66]

Then use the prepared sample from above to scoop up the CVD graphene in DI water to form the graphene to TMD contact. Electron beam lithography and oxygen plasma etching were used to pattern the graphene electrodes. Depositing Metal electrodes, consisting of 10 nm of Ti covered by 40 nm of Au, were fabricated to electrically wire up the graphene electrodes using standard electron beam lithography (EBL) and electron beam deposition. Ionic liquid gate electrodes were also fabricated in the same step. A same procedure of the dry transfer process used to passivate the WSe_2 channel with a clean h-BN flakes is also presented.

In the part of graphene contacted device, we are doping the graphene contact in order to reach barrier-free contact. The electrostatic doping method (Ionic liquid), and air stable molecular doping method (BV, F4-TCNQ) are then introduced, where (1) Ionic liquid for electron and hole doping, (2) F4-TCNQ for hole doping, and (3) BV for electron doping are addressed following:

2.4.2 Doping method: Ionic Liquid

In order to achieve the low resistant contact of the graphene contacted device, we first use ionic-liquid (IL) gate as electrostatic doping on graphene electrode. The Ionic-liquid (DEME-TFSI) we purchased from Sigma Aldrich supplies was then carefully applied one small droplet onto the devices using a micromanipulator under an optical microscope. From the transfer characteristic of graphene FETs, when applying varies voltage on the IL gate electrode, we observed the Dirac point was then shifted accordingly indicating the fermi level of graphene can be significantly modified by IL-gate. The working principle will be addressed in the detail in the chapter 3

2.4.3 Doping method: BV and F4-TCNQ

Two types of solution, Benzyl Viologen (BV) and F4-TCNQ, for the surface charge transfer doping methods is introduced. Both solutions contain chemical substances or molecular which can carry charges. When applying a solution to a device, those charges will be directly in contact with the surface of the device (channel or contact region,) resulting in electron doing (BV) and hole doping (F4-TCNQ.) The preparation for both solutions are as following.

For F4TCNQ doping method, weight 3 mg of F4-TCNQ powder and mix with 3 ml of chloroform, until it is fully dissolved or saturated, the color of the solution should look lightly yellowish and green. To apply the F4-TCNQ to the device, we first put one drop of F4-TCNQ solution on the top of the device area, and air dried. Notice, the crystallizing could occur when it is air dried. Notice with applying few more drops resulting in higher the doping level (hole density) on graphene; however the chance of getting denser crystallizing on device is high when applying more F4-TCNQ which can severely damage the device. To remove the F4-TCNQ,

rinsing the device with isopropanol and N_2 blow dry. Also the post- annealing with 250^{o}C for 30 minutes is recommend in order to remove the F4-TCNQ residue on the surface of the device.

For the BV doping method, the BV mixture solution is introduced and prepared as follows. It contains four substances: DI water, BV (powder), Toluene, and $NaBH_4$ (powder). We first prepare 2.5ml of DI water, and 50 mg of BV, 2.5ml of Toluene, and 47 mg of $NaBH_4$ in clean containers separately. It is necessary to mix each substance with the following procedure in order to get the correct chemical reaction for the final BV mixture solution.

First, pour 2.5ml of DI water into the container which contains 50mg of BV (powder), and apply a gentle shack until it is complete dissolved; second, gently pour 2.5ml of Toluene into the container which contains the mixture of 2.5ml of DI water and 50mg of BV. The separated layer should appear as DI water/BV mixture on top and Toluene at bottom. Third, gently pour the $NaBH_4$ powder into the solution mixture which contains DI water/BV mixture/Toluene, and the chemical reaction will appear once the $NaBH_4$ powder in touch with the solution mixture (DI water/BV mixture/Toluene.) The color of the final mixture will then change to dark purple (Fig. 2.9(a)). Next wait 18 to 24 hour until the solution is completing the chemical reaction, now the BV mixture solution should be appeared as the bottom (yellow BV mixture as a final solution) and DI water on the top, then carefully extract the bottom yellow BV mixture part and transfer to a clean container by using the pipet for the further usage (Fig. 2.9(b)).

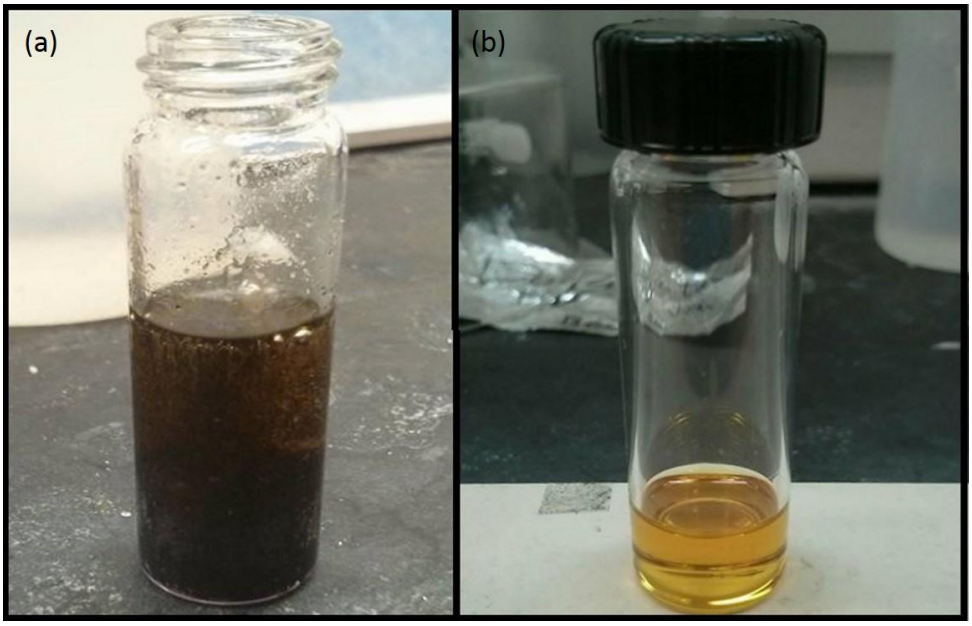


Figure 2.9 (a) Shows the chemical reaction right after pour the $NaBH_4$ powder into the solution mixture of DI water/BV mixture/Toluene. (b) The Final BV mixture extracted from the (a) after 18-24 hour chemical reaction time.

To apply BV solution to the device, first put one drop of BV solution, wait for 30 seconds then spin coated with the 1500rpm spin rate for 35 seconds. To remove the BV layer, rinse the device with isopropanol and N_2 blow dry.[67] Again, the further annealing with 250^oC for 30 minutes is recommended in order to remove the F4-TCNQ residue on the surface of the device

2.4.4 Fabrication of multilayer TMD field-effect transistors (FETs) with 2D/2D contacts and h-BN encapsulated channel and For the Synthesis of bulk crystals of undoped WSe_2 and $MoSe_2$, Nb-doped WSe_2 and MoS_2, and Re-doped WSe_2.

The flow chart (Fig. 2.10) of Fabrication of ultrathin TMD field-effect transistors (FETs) with 2D/2D contacts and h-BN encapsulated channel and Fabrication of TMD FETs with 2D/2D contacts and hBN encapsulated channel. **a(I-II)** is showing as following. Exfoliate atomically thin TMD channel material onto a PDMS stamp and stack it on top of a thin bottom h-BN (10 - 30 nm) pre-transferred onto the SiO_2/Si substrate. **a(III- IV)** Exfoliate and transfer a thin top h-BN crystal (5 - 20 nm) to encapsulate the TMD channel. **a(V-VI)** Stack degenerately doped TMD electrodes on top of the exposed contact areas of the TMD channel to make

2D/2Ddrain/source contacts. Noticed gently heating procedure is applied after every dry transfer steps which heat substrate is heated from room temperature to 65 ^{o}C for 15-20 minutes to improve the interface bonding and preventing shifting of the stacked flakes. **a(VII)** Deposit metal electrodes on top of doped TMD drain/source contacts. **b(I)** Degenerately doped TMD exfoliated on SiO2/Si substrate. **b(II)** TMD drain/source electrodes defined by EBL and SF6 dry etching. **b(III-IV)** Pick-up and transfer of the degenerately doped TMD electrodes for 2D/2D contact fabrication. 4 Polycarbonate (PC)/PDMS double layer is used for the TMD electrode pick-up and subsequent transfer process.

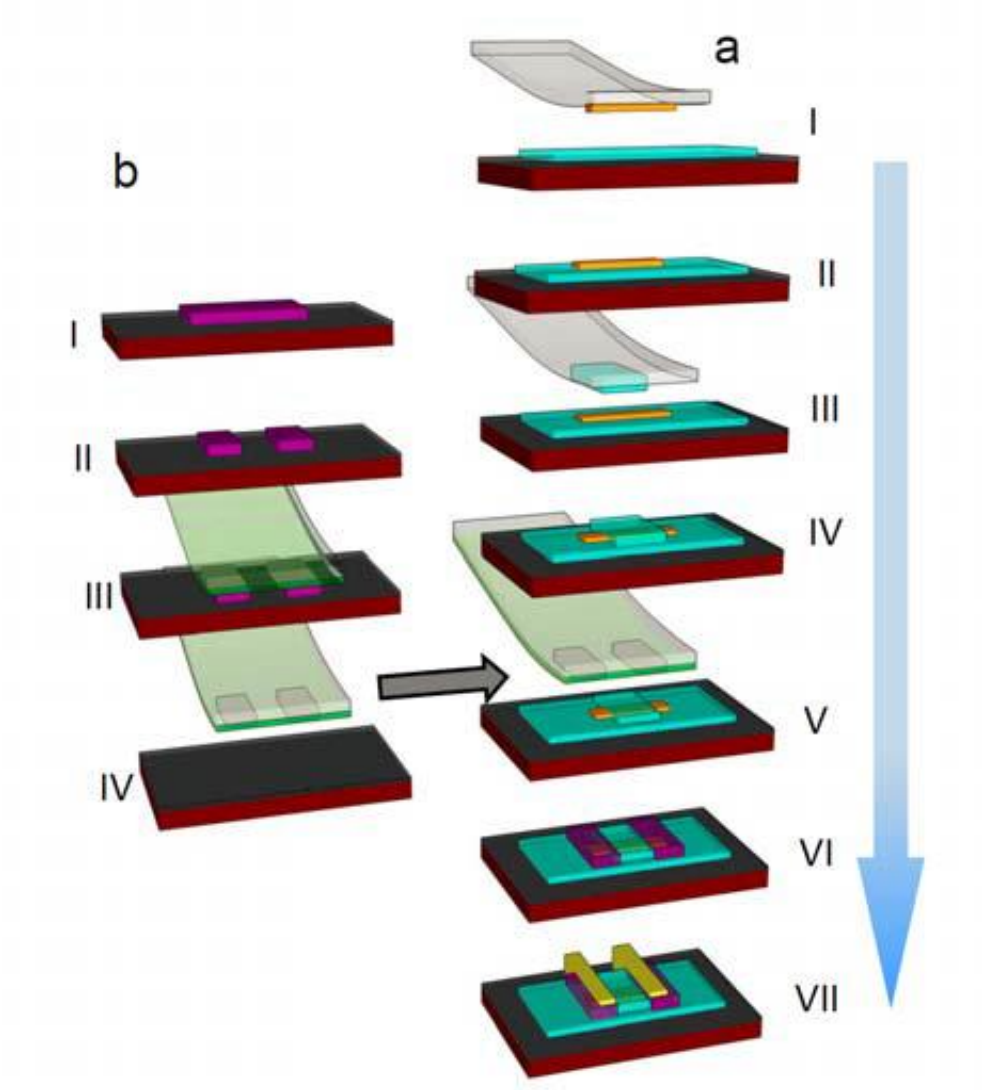


Figure 2.10 Shows the process flow of the device fabrication. Thin h-BN crystals (10 - 30 nm thick) were produced from bulk h-BN crystals by a mechanical cleavage method and subsequently transferred onto degenerately doped silicon substrate covered with a 270 - 290 nm-thick thermal oxide layer. Atomically thin flakes of undoped TMDs were exfoliated from bulk crystals onto a PDMS stamp. Using a home-built precision transfer stage, undoped few-layer TMD flakes used as the channel were subsequently transferred onto a selected thin h-BN crystals on the SiO_2/Si substrate. To passivate the TMD channel, a second thin h-BN crystal is exfoliated to a PDMS stamp and subsequently transferred onto the few-layer WSe_2 flake to cover its middle section while exposing its two ends for electrical contacts. To make 2D/2D contacts, degenerately doped TMDs are exfoliated on to Si/SiO_2 substrates, patterned into drain/source electrodes by electron-beam lithography and SF6 dry etching, and transferred to the two exposed ends of the TMD channel as drain/source contacts using a pick-up method. Alternatively, thin flakes of degenerately doped TMDs can be exfoliated onto PDMS stamps and transferred to the two exposed ends of the TMD channel as drain/source contacts, especially for long channel devices. To improve the interface quality between the h-BN and TMD channel as well as between the doped TMD drain/source contacts and TMD channel, a mild annealing step was carried out. The dimensions (e.g. the sample thickness) and the surface quality (e.g. the cleanness and smoothness) of the h-BN substrate and TMD channel were characterized by Park Systems atomic force microscopy (AFM) in the non-contact mode after each annealing step. Metal electrodes, consisting of 10 nm of Ti covered by 40 nm of Au, were fabricated to electrically wire up the degenerately doped TMD drain/source electrodes using standard electron beam lithography (EBL) and electron beam deposition.

We also fully characterize the surface of the flake after each transfer step by using AFM in order to secure the interface quality of the device, the one example is showing below. Notice in the Fig. 2.11 (a), and (b) shows overlapping region, the black dashed line, indicate the interface of the 2D/2D contact region is bubble free leading to the good performance of device.

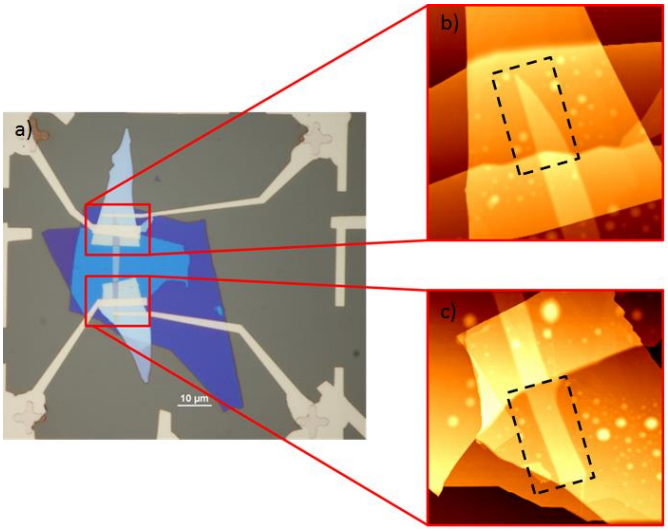


Figure 2.11 (a) Shows optical image of the device where (b), (c) shows the AMF image at the contact overlapping region for top and bottom contact of the device respectively, note the AFM image was taken before metal deposition.

2.5 Others

2.5.1 Electron beam lithography

Electron beam lithography (EBL) is the most well-known and powerful technic to fabricate nanoscale devices, such as field effect transistors. The configuration of whole system is attached to the standard SEM showing as in Fig. 2.12

Figure 2.12 The complete SEM system (Hitachi S-2400) with EBL attachment.

For standard procedure of EBL, we first deposit the electron resist (PMMA) as a mask for the patterning purpose on the substrate. One layer PMMA is commonly used in most cases; however, we spin coated two types of the electron resist PMMA 495KA4 and 950K-A2 (MicroChem Inc., 495/950 represents different molecular weight; A2/A4 represents concentration) in which 495A4 as bottom layer, 950-A2 as top layer for the ease of lift-off procedure after metal deposition. The simple cartoon (Fig. 2.13) explains the concept of lift off process after coating multilayer of PMMA.

The Spin coating procedure is presented as two drops of PMMA on the prepared substrate with the 4000rpm in 45 seconds to thinner the layer, for thickness of the PMMA is

around 80nm and 220nm for PMMA 950-A2 and 495-A4 respectably. (Cited the MicroChem). Then 180 C baking on the hotplate for 5 min after each coating procedure. Next, the silver paint, acts as the focus point, will be cautiously put on the side of alignment mark where the target WSe_2 sample are nearby. Before doing electron beam lithography, the electrodes have to be completely designed and runs on the NPGS Designcad software. NPGS software is the one which we used to control the electron beam and SEM system (Hitachi S-2400).

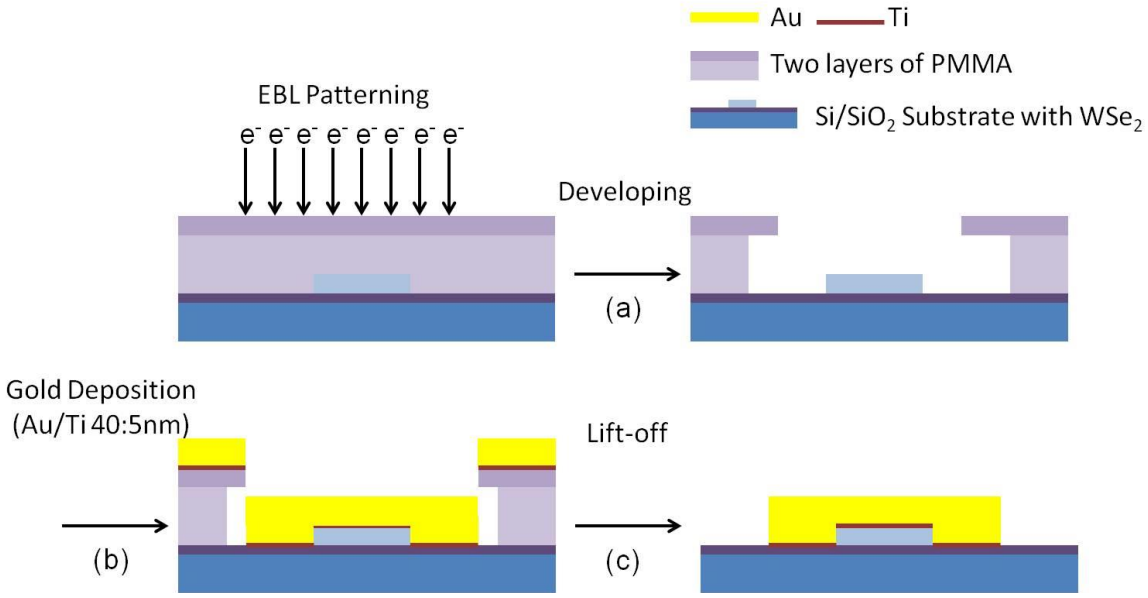


Figure 2.13 The simple cartoon flow chart indicates purpose of applying two layers of PMMA, since the bottom layer has smaller molecular weight (495-A4), the cross-link of the PMMA will be much easier to be broken by electron resulting in wider area or so called under-cut after developing; therefore, it will be much easier to do the lift-off processes. (a) Shows the developing process; (b) depositing Au/Ti as the contact electrode; (c) Immerse into acetone for the lift-off process (PMMA can be removed by acetone.)

Being familiar with operating SEM would be one of the most important prerequisites to write the proper patterns for electrodes. The parameters such as dose and current, of course, are critical to write the designed patterns. Normally, the current keeps around 12.0 pA to write narrower electrodes and the area dose is set to be 260uC/cm^2. Followed by developing process using the mixture chemicals of MIBK/IPA 3:1(original developer for PMMA) along with very small amount of MEK, in which we use the portion of 1 tube of (MIBK/IPA mixture) with one

drop of MEK to enhance the resolution and sharpness of the pattern for 70 second with sonication 10 second if needed, rinse with IPA, followed by N_2 blow dry. Fig. 2.14 shows one of the example after completing lithography process and developing.

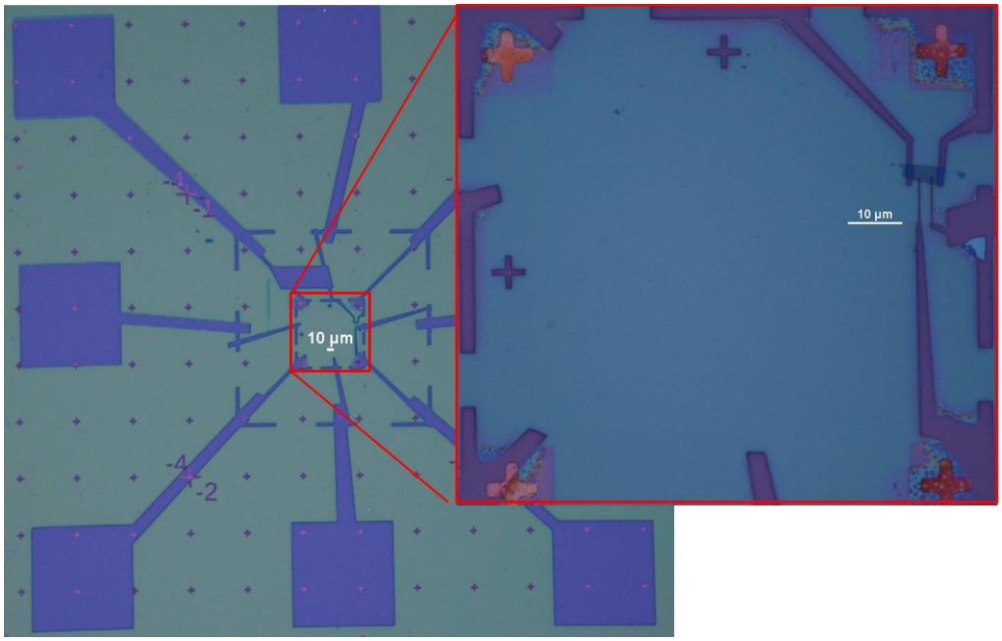


Figure 2.14 The Optical microscopy image is taken after developing procedure (Fig. 2.13(a)). The 10X picture (left) is showing the whole device along with the enlarged picture (right, taken under 100X magnification). Under the 100x mag. image, the purple color contrast indicates the bare substrate after developing procedure also showed EBL patterning area (electrode) where touch the WSe_2 sample, and blue color contrast is showing PMMA coverage. In this image, we designed 4 electrode for the four probe measurement purpose.

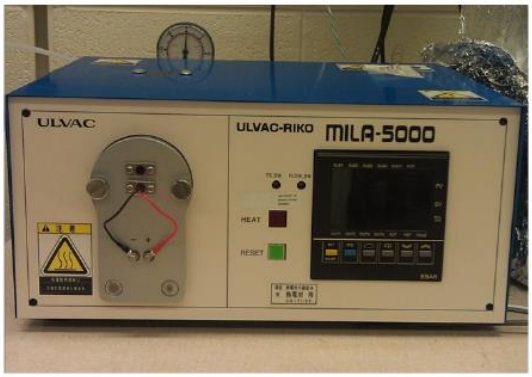
2.5.2 Metal deposition

In order to be able to do the measurement on the WSe_2 FET, evaporation with one layer of Ti and Au was used to fabricate the FET devices as the final step of the fabrication in which is one of the most critical step. The whole set-up including chamber, diffusion pump and thickness monitoring of crystal. The deposition rates was set to be 1A/s for both Au and Ti. In our case, the required thicknesses of Au and Ti are 40 nm and 10 nm respectively. While it is processing, the equipment is first pumped down to the required pressure (< 1x10-6 Torr) using mechanical pump follow with diffusion pump in order to prevent the damage on the diffusion pump. Whenever the

liquid nitrogen is used, the pumping efficiency of diffusion pump will be improved from 4 hours to 2 hours. In addition, cleaning up the chamber and sample holder using IPA after single use definitely increases the pumping speed. It is also necessary to notice the life time of crystal sensor, in which is critical to monitor the deposition rate and thickness.

2.5.3 Annealing

The setup of the annealler is showing in Fig. 2.15 with desired programs for different purposes. The program detail will be introduced as follows.



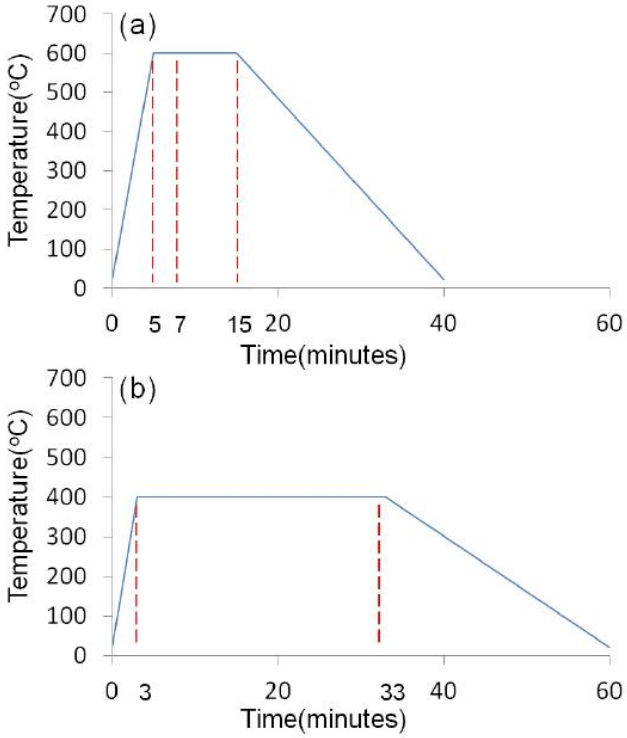


Figure 2.15 The annealler set on the left, two program has been set up for two purposes, (a) for the cleaning bare substrate; (b) for the purpose of improve the contact at transferred CVD graphene to TMD interface, also could be used for doping graphene contact.

The annealing procedure we are using for the substrate cleaning is as following. First, loading the sample into to chamber with the pumping chamber down to the vacuum then purging the chamber with the forming gas($Ar:H_2$) for at least three. Second, switch on the heating program (Fig. 2.15 (a)), it will heat up from room temperature to 600^oC in 5 minutes, then at stay

constant temperature of 600 ^{o}C for 10 minutes during the 10 minutes slowly flow in the forming gas (Ar/H_2) into the chamber for two minutes, after the 10 minutes heating it will then quench it down back to room temperature. Another program was used for improvement of the interface contact in between graphene sheet of the device which we suspected the interface impurity was introduced during the wet-graphene transfer cause the difficulty of getting good result. It begin with the same purge procedure then the system will heat up to 400 ^{o}C in 3 minutes, stay constant temperature 400 ^{o}C for 30 minutes, then quench down to the room temperature, No forming gas flow into the chamber (In this case the annealing procedure might cause slightly doping effect on graphene)

CHAPTER 3 HIGH PERFORMANCE TMDS FETS DEVICES ENABLED BY IL GATING WITH GRAPHENE CONTACTED ELECTRODE

3.1 Background

The Layered TMDs have attracted much attention in the past few years by its promising property of TMDs, such as for flexible electronics and optoelectronics applications. It has many graphene-like properties such as high intrinsic mobility, mechanical flexible, chemical and thermal stable, and has significant advantages of a substantial band gap.[68] TMDs as the channel material for field-effect transistors (FETs) with its atomically thin property, it immune to short channel effects.[69] Moreover, the free dangling bonds and the pristine surfaces of TMDs reduce surface roughness scattering and interface charge traps. An example, MoS_2, has been probably the most extensively studied among the other TMDs due to the availability of large natural molybdenite crystals from mining sources.[70] In additional, the MoS_2 among the several other semiconducting TMDs such as $MoSe_2$, WS_2 and WSe_2 with different band gaps, structures and charge neutrality levels may show other offer to additional distinct properties.[68,71] However, the number of researches on TMDs other than MoS_2 is still unexplored.[72-81] Among these studies, back-gate single layer WSe_2 FETs with surface doping have already observed a high field-effect mobility[75] reaching ~140 $cm^2V^{-1}s^{-1}$at room temperature, which is higher than most of the reported MoS_2 FETs.[82-86] For Bulk WSe_2 at room temperature, the high intrinsic hole mobility up to 500 $cm^2V^{-1}s^{-1}$ was also observed.[77] Moreover, WSe_2 is also more resistant to environments such as the oxidation and humid environments than other TMDS.[77,87] However, the major challenge for most of TMDs-based electronic devices is to form a significant Schottky barrier (SB) at contact region, For the WSe_2, it tends to form SB with most metals that commonly used for making electrical contacts.[75,80] Since the low-resistance ohmic contacts are needed for

studying the intrinsic transport properties of the channel material, also to improve device performance for practical applications. The typical two approaches to achieve low resistance contacts between a semiconductor to metal contact are (1) by using degenerate doping methods at the contact regions to thin the SB width, and (2) Using high or low for work function metal material for lowering the SB height for n-type semiconductors and p-type semiconductors respectively. Low-resistance contacts have been reported by surface doping of WSe_2 such as using NO_2 and high K in order to reduce the SB thickness, or by using low work function contact metals such as Indium for lowering the height of the SB to the conduction band[75,77,79]; however, NO_2 and high K doping is not suitable for practically application since its instability in air. Also, the Indium adheres quite poorly to substrate and also it is thermally instable due to its low melting point of 426K.[77] In our previous work,[2] we have presented the significant improvement for contacts of few-layer MoS_2 FETs devices by significantly reducing the SB with using an Ionic Liquid (IL) gate;[81] however, the improvement of charge injection efficiency is still limited by the Schottky barrier height which further indicates it is not a suitable method for practical application of low resistance ohmic contact of TMDS FETs.

The Schottky barrier height could be reduced by suitable metal for contact material, as mentioned above, by using the low work function metal or the high work function metal. However, it has been proved it still challenging to find metals with a proper work function that also has high conductivity and a high chemical, thermal and electrical stability. In additional, the suitable work function of metal for lowering the SB may be significantly reduced by Fermi level pinning.[69,82] with the proof from recent theoretical study, it shows that partial Fermi level pinning is presenting at the metal to TMDs contacts regions for a variety of metals.[88]

3.2 New strategy for high performance devices

As the challenge is well addressed in the previous section, we further investigate possible new methods in order to offer true ohmic contact electronic device, two main methods are then developed. In this chapter, we offer the first method where to utilize the application of graphene as a band gap tunable material as a contact electrode in the TMDs FETs devices, resulting in overcome the limitations of metal electrodes to few-layer WSe_2 FETs.

It is well known that graphene is desirable for flexible electronics applications with its mechanically strong, flexible and thermally stable property and many others. Moreover, the work function of graphene is tunable by using chemically or electrostatically doping method which in principle can be used to minimize the SB height at the graphene to semiconductor interface.[89,90] With this transport advantage of graphene, we here offer the first method to reduce S.B by using the extremely large electric double layer (EDL) capacitance of an IL gate, the work function of graphene at the graphene to WSe_2 interface can be modified within the large range. As a result, we have formed for the first time, the single WSe_2-based FETs device for both n- and p-type FETs that shows the low-resistance contacts and high mobility. Even though devices based on graphene-TMDs heterostructures have been reported previously,[91-93] the working principle of the WSe_2 FETs with lateral graphene contacts is qualitatively different from the previously reported graphene-based field-effect tunneling transistors (FETTs) and vertical field-effect transistors (VFETs). Also, the transport in FETTs and VFETs based on graphene to TMDs heterostructures is modified by the vertical transport barrier at the graphene to TMDS junctions, the graphene to TMDs junctions in our devices serve as the drain and the source contacts to lateral WSe_2 FETs. I would like also to emphasize that IL gating is important to achieve sufficiently large

modulation of the graphene work function in which is needed to achieve the low resistance contacts on both the valence band and conduction band of WSe_2.

3.2.1 Graphene Contacted TMDs FETs Device Fabrication

The fabrication of graphene contacted WSe_2 FETs devices will be addressed in this section. Atomically thin WSe_2 flakes were first exfoliated from a bulk single crystal and transferred onto silicon substrates covered with a 290 nm thick thermal oxide layer[81,94-96] with conventional exfoliation method following by the optical microscope to identify thin flakes, then further characterized by atomic force microscopy (AFM). We then mainly focus on few-layer samples of 4-12 layers with the range of corresponding thickness of 3-8 nm. It is believed that only few layers can be produced more easily and sustain larger drive currents than single layer also maintaining a relatively large ON/OFF ratio and a small c-axis interlayer resistance in comparison to thicker samples. [97-99] Next, transfer a thin hexagonal boron nitride (h-BN) crystal (10–50 nm thick) onto a few layer WSe_2 flake to cover its middle section for preserve the channel property by the dry transfer method where was discussed in the chapter 2. Passivating the WSe_2 channel by h-BN enables us to tune separately the SB height at the graphene drain/source contacts using the IL gate and the chemical potential of the channel using the Si back gate. The reason of using h-BN as the device channel passivation layer is due to its atomically smooth surface and chemically inert, relatively free of charged impurities and charge traps properties.[100-102] Next, we transfer CVD grown monolayer graphene on top of the h-BN covered WSe_2 device. Then fabricate metal electrodes which consisting of 10 nm of Ti covered by 40 nm of Au, by using standard electron beam lithography (EBL) and electron beam deposition.[103] Also a large metal electrode on the side of the device was fabricated to serve as an IL gate electrode. Finally, we removed section of the graphene which is on top of the h-BN

covered WSe_2 channel area by EBL patterning follow with oxygen plasma etching. For the top gating, a small droplet of the DEME-TFSI IL (Sigma Aldrich 727679) was carefully deposited onto the devices by using a micromanipulator under an optical microscope, covering the WSe_2 devices and large gate electrodes.[81]

3.2.2 Working principle

In Fig. 3.1(a.) It shows a schematic illustration and in Fig. 3.1(b) a micrograph of a WSe_2 FET device with graphene where white dashed lines indicate the CVD graphene. In Fig. 3.1(c), it shows an AFM image of black solid lines boxed in Fig. 3.1(b), which consisting of the h-BH covered channel, graphene drain and source contacts, and a part of the Au leads contacting the graphene electrodes. As showed in the Fig. 3.1(c) the large clean part of the graphene -WSe_2 drain area at drain and source contacts with some bubbles, with a relatively low RMS roughness of a nanometer, indicating a high quality of the graphene/WSe_2 interface.

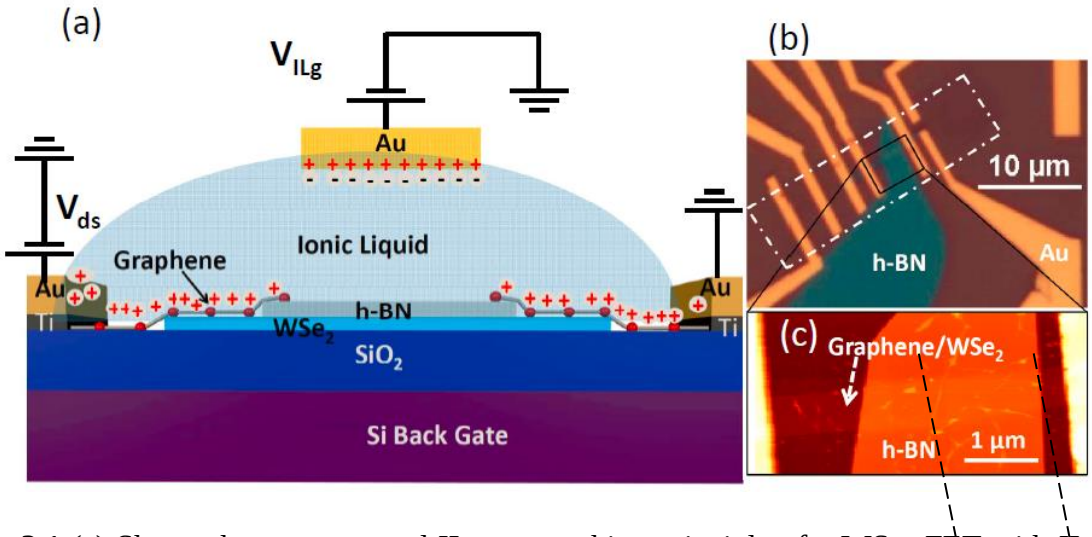


Figure 3.1 (a) Shows the structure and IL gate working principle of a WSe_2 FET with IL-gated graphene contacts. (b) Optical micrograph of a typical WSe_2 FET with graphene electrodes before applying the IL where the contours of the graphene are marked by white dashed lines Note, the graphene is then etched out by oxygen plasma at the top surface of h-BN to WSe_2 overlapping region. (c) AFM image of the device region enclosed in the black box in (b). The black dashed line indicate the edge of the graphene after oxygen plasma etching, the scale bar is 1 µm.

The few wrinkles observed in the graphene / WSe_2 overlapping contact areas in Fig. 3.1(c) which are not expected to have a significant impact on the overall contact quality. The Electrical properties of the devices were measured by a Keithley 4200 semiconductor parameter analyzer in a Lakeshore Cryogenic probe station, also in order to remove additional moisture through the fabrication process thoroughly, we place the device under high vacuum (~1×10^{-6} Torr) for 48 hours after placing the IL droplet to the device, which turned out to be important for preventing the formation of chemically reactive protons and hydroxyls through the electrolysis of water.[81,106]

To address the working principle of IL gating, is shown in the Fig. 3.1(a), negative ions in the IL accumulate near the gate electrode and positive ions accumulate near the WSe_2 channel due to a positive voltage V_{ILg} is applied to the IL gate electrode, reverses when a negative voltage is applied to the gate. In both cases, EDL (electric double layers) form at the interface.[81,107] The electrical transport measurement of the device cannot be carried out at room due to the possibility of chemical reactions involving the IL at high voltages to avoid the damage to the device. The measure or the working temperature in this study is at the range between 77K and 180K since the electrochemical stability of the IL increases with decreasing temperature so that larger IL gate voltages can be applied without causing chemical reactions at lower temperatures.

First, the devices had been quickly cooled from 230 K to below 170 K at fixed IL voltage, with the back gate being grounded. Below the freezing point of the IL at ≈200 K, all the mobile carrier in IL will be locally frozen thus, the carrier density induced by the presence of positive or negative ions, which preferentially enriched the vicinity of WSe_2, remained practically

constant.[21] Measuring the electrical property of IL-gated devices below the freezing point of the IL also eliminates possible coupling between the Si back and IL gate.[81,98]

3.2.3 Ionic Liquid gating effect on graphene

The Fermi energy of a graphene monolayer changes as $\Delta E_F = (h/2\pi)\, v_F\, (\pi\, n)^{1/2}$, where $v_F = 1.1\times10^6$ m/s is the Fermi velocity and n is the carrier density. The Fermi energy of a graphene monolayer is expected to be tunable by up to ±1.5 eV using an IL gate due to its extremely large electric double layer (EDL) capacitance. Such a wide range of Fermi energy tunability in graphene enables us to continuously change the work function of graphene from ~ 3 eV to ~6 eV, opening up the possibility of controllably making low-resistance Ohmic contacts with a vanishing or even negative Schottky barrier for both the electrons and holes in most semiconducting TMDS. In addition to lowering the contact barrier at the graphene/TMDS interface, the high carrier density induced by the IL gating is also expected to reduce the sheet resistance of graphene.

3.3 Device Performance

Among several devices, we have measured three different kind of devices that one had bare channels without covering with hBN protection layer., one had its channel covered by a 50 nm thick Al_2O_3 layer, on had h-BN channel passivation. With consistent promising results were observed in all devices, the two h-BN covered WSe_2 devices showed the best performance, which can be attributed to the excellent interface quality between WSe_2 and h-BN.

3.3.1 Electrical transport properties of bear WSe_2 device

As shown in Fig. 3.2(a) and 3.2(b,) the output characteristics of an 8 nm thick bear, i.e. no passivated layer on WSe_2 channel with IL-gate graphene contacts shows Ohmic behavior. The highest current in this device approaches 200 μA/μm at 4.0 μm channel length at the back-gate

voltage V_{bg} = 100 V, bias voltage V_{ds}= -5 V, with IL gate voltage V_{ILg} = -4.5 V. And the ON/OFF ratio in the bear device is substantially reduced due to the IL-gating of the channel[2] as well. Especially at high IL-gate voltages, as seen in Fig. 3.2(c). Figures 3.2(e), (f) show the field-effect mobility of the bear WSe_2 device for both the hole and electron channels.

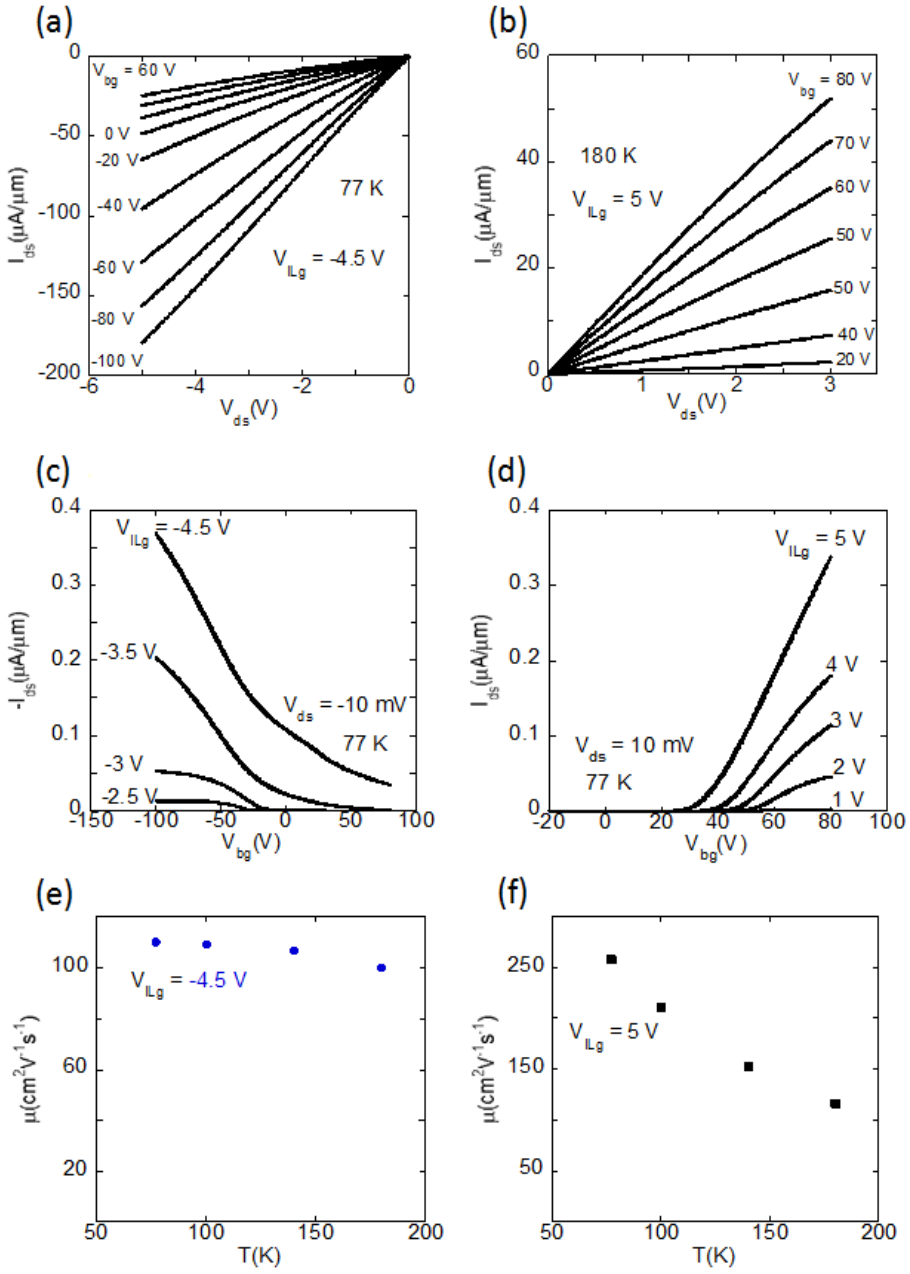


Figure 3.2 An 8 nm thick WSe_2 FET device with a channel length of L = 4 μm and IL-gated graphene contacts. (a) and (b) shows output characteristics for the hole and electron channels. (c)

and (d) shows transfer characteristics for the hole and electron channels. (e) and (f) shows field effect mobility extracted from the low-bias (V_{ds} = 10 mV) transfer characteristics for the hole and electron channels.

3.3.2 Electrical transport properties of WSe_2 device with Al_2O_3 passivation.

For the sake of comparison, we then measured a graphene-contacted WSe_2 device where the device channel is passivated with 50 nm of electron beam deposited Al_2O_3. Figures 3.3(a) and 3.3b show the transfer characteristics of the device, while the graphene contacts have been either highly "p-doped" by applying a very high IL gate voltage of -6 V or "n-doped" by applying an IL gate voltage of +6V.

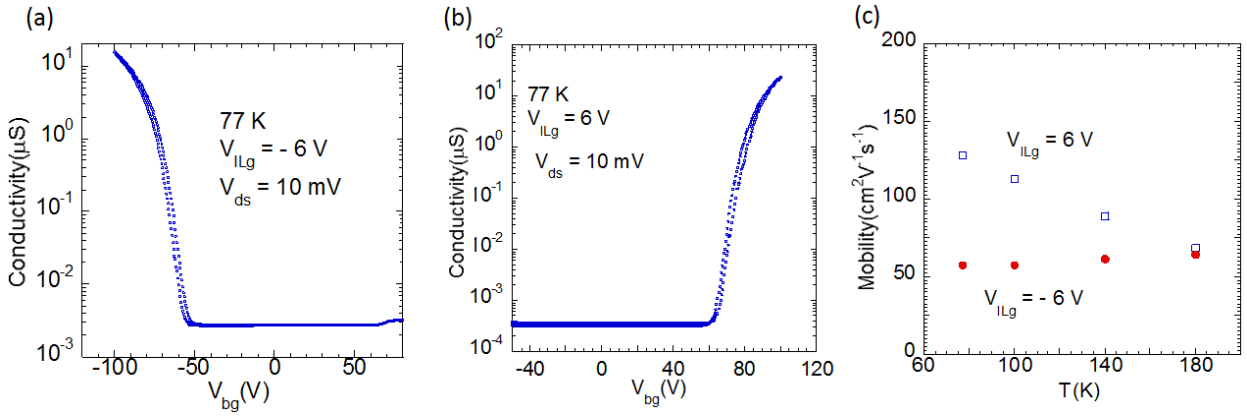


Figure 3.3 (a,)(b) Show transfer characteristics of a 7 nm thick WSe_2 FETs with ionic-liquid gated graphene contacts, measured at V_{ILg} = -6 V (hole channel) and V_{ILg} = 6 V (electron channel). (c) Field-effect mobility of the devices in the hole- (V_{ILg} = -6 V) and electron-doped (V_{ILg} = 6 V) regions.

3.3.3 Electrical transport properties of WSe_2 device with hBN passivation

In Figure 3.4(a,) it shows the transfer characteristics of a 6 nm thick h-BN passivated WSe_2 sample and a channel length is 4.8 μm, measured at room temperature at V_{ds} = 0.1 V before the IL has been deposited. The clear ambipolar behavior was observed in this device with relatively low drain-source current for both the p- and n- channels, indicates the presence of the significant SBs in both the valence and conduction band regions of WSe_2 channel. So that both electron and hole injection is accomplished either via thermal excitation across the SB or

tunneling at the band edge, or with the combination of first two mechanism (thermally assisted tunneling.)

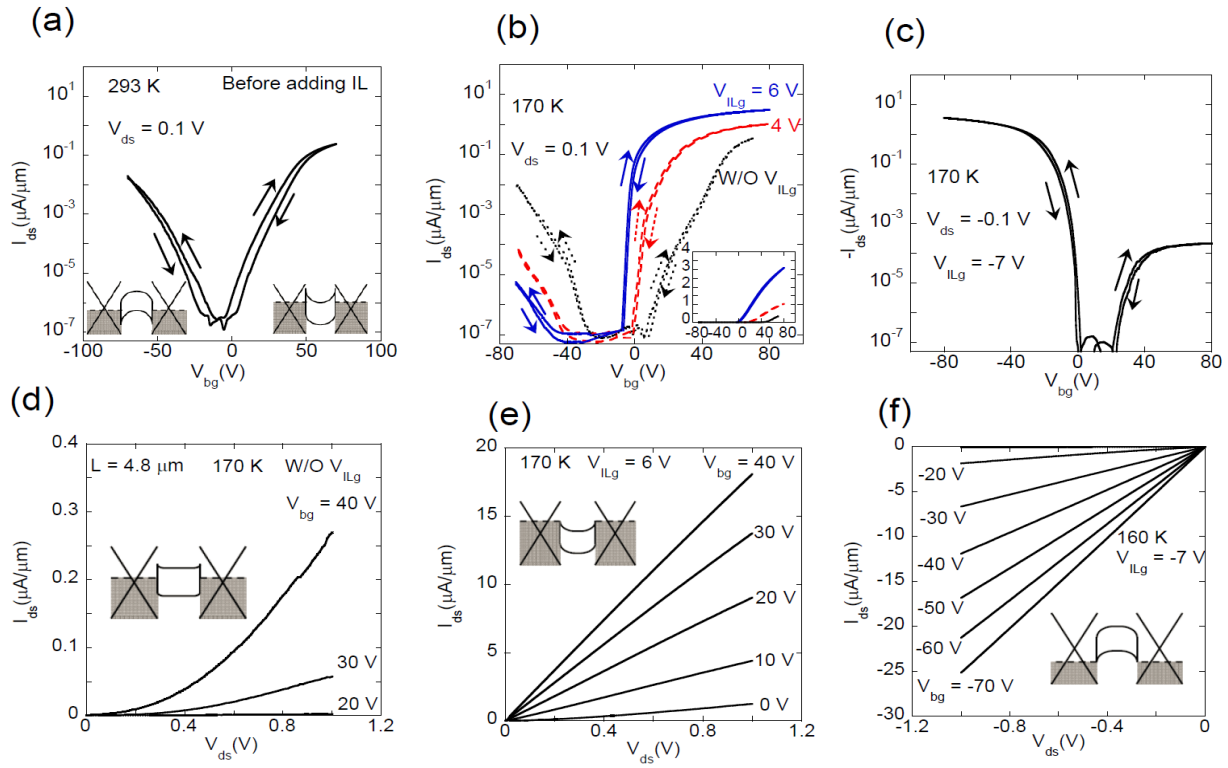


Figure 3.4 Transfer and output characteristics of a 6 nm thick WSe_2 FET device with graphene contacts and a 4.8 μm long channel passivated by h-BN. (a) band diagram and Transfer characteristic of the device that measured at 293 K with V_{ds} = 0.1 V without IL. (b) Transfer characteristics at V_{ds} = 0.1 V with IL gate voltages of V_{ILg} = 0, 4, 6 V, which V_{ILg} was applied when the sample was cooled down from 230 to 170 K. The inset shows the same data on a linear scale. (c) Transfer characteristics at V_{ds} = -0.1 V with IL gate voltages of V_{ILg} = -7 V, which V_{ILg} was applied when the sample was cooled down from 230 to 170 K. (d-f) Output I-V characteristics of the device at zero applied IL gate voltage, different back-gate and IL gate voltages, measured after the device has been cooled down from 230 K to 170 K without applying IL gate voltage. The insets in (a), (d), (e) and (f) show schematically the SB height and width band diagram at various IL and back gate voltages.

Consequently, electrons (holes) are preferably injected into the conduction (valence) band as the back-gate induced band bending to reduce the SB thickness. As the back-gate modifies the graphene carrier density which shifts the Fermi level graphene, resulting in lowering the SB height at high positive (negative) gate voltages. This process demonstrates in

the inset of Fig. 3.4(a) which further reduce the SB height of at the graphene to WSe_2 contacts region for the intrinsic performance of WSe_2 as a FET channel material.

To minimize the SB height and thus the reduce contact resistance, we applied large positive (negative) IL gate voltages to the graphene contacts for optimizing the electron (hole) injection to WSe_2. In the Figure 3.4(b), it shows the transfer characteristics of the device measured at 170 K which is below freezing point of IL and in the Si back gate configuration for different IL gate voltages applied during cooling down from 230 K to 170 K. The result with excluding the channel effect from the IL gating since the WSe_2 channel is protected from direct contact with the IL by a h-BN passivation, so that difference in the transfer characteristics for different V_{ILg} is mainly from the IL-gate tuning of the graphene to WSe_2 contacts. Without applying a V_{ILg}, the transport of the device shows a similar ambipolar behavior with comparable electron and hole currents of the device with covering IL, indicating the effect from IL to the device can be excluded showing in the later section 3.3.6. As applying the V_{ILg} up to V_{ILg} = 6 V, the ON-current for the electron channel, measured at V_{bg} = 70 V, increases by an order of magnitude to 3 μA/μm, while the hole current measured at V_{bg} = -70 V decreases by over three orders of magnitude from 10^{-2} μA/μm to below 10^{-5} μA/μm. The performance which shows in ON/OFF ratio of the device > 10^7 for the electron channel, and On/OFF ratio less than 10^2 for hole channel with V_{ILg} = 6 V measured below the IL freezing point. This shows it associates with opposite trends for changing the SB height to the conduction bands and valence bands, where when apply V_{ILg}, it modifies the carrier density that tuned the Fermi level in the graphene contacts. When increases positive IL gate voltage, the Fermi level in graphene moves up, resulting in decreasing (increasing) the SB height for the conduction (valence) band. Also, the threshold voltage decreases with increasing IL gate voltage, showing in the inset of Fig. 3.4(b.)

This attribution of reducing SB height for the conduction band is due to higher V_{bg} is needed to overcome a larger SB height for electrons to inject into the conduction band, mainly through the band bending. It is also shown that the charge trapped from SiO_2 substrate causes the hysteresis in the transfer characteristics showing in Figure 3.4 (a.) Below 170K the charge trapping is mainly suppressed (see Figure 3.4(b)),[46-48] resulting in less hysteresis. In Figure 3.4(d,) the I-V output characteristics shows the strongly non-linear behavior for the device cooled down to 170K without apply IL gate voltage, indicating the presence of a significant SB, whereas the I – V output characteristics of the same device, shows strong linear behavior for at all back gate voltages above threshold voltage indicating the significant reduction of SB at device contact applying in Figure 3.3(e,) V_{ILg}= 6 V. Moreover, without applying IL gate, the resistance is over 2 orders of magnitude larger than for V_{ILg} = 6 V of the device which the resistance was calculated from of the I_{ds} - V_{ds} characteristics slope, in the low-bias region at V_{bg} = 40 V. When measuring at V_{ds}= 1V and V_{bg}=40 V without IL gate voltage, The ON-current (0.27 µA/µm), is significantly smaller (67 times) than the ON-current (18 µA/µm) for V_{ILg}=6 V. Both results shows and provides evidence which applying large positive IL gate leading to reduce the contact resistance for the electron channel, most likely to lowering the SB height consist with our prediction showing in schematically in the insets of Figures 3.4 (d) and 3.4 (e.)

Since the Fermi level of graphene at contact is close to the middle of the WSe_2 band gap, the significant SB is observed without applying IL voltage to the device. Applying IL gate = 6V, the Fermi level of graphene shifts close to the conduction band edge, leading to the low SB. Also from the I-V output data shows at V_{ILg} = 6 V, V_{bg} = 40 V and V_{ds}= 1 V still has not reach saturation region, indicating that higher ON-currents are possible, showing in section 3.4.4. From Figure 3.4 (c) and 3.4 (f,) it shows the transfer and output characteristics on the same devices at

V_{ILg} = -7 V. When the graphene to WSe_2 contacts are gated by a large negative IL gate voltage, the device exhibits p-type conduction with a high current ON/OFF ratio about 10^7. In this case, the hole injection of WSe_2 FETs device at the contact is significantly reduce the SB for the valence band. As apply large negative IL gate the Fermi level of the graphene has been lowered and shifts close to the valence band edge, as showing in the inset of Fig. 3.4(f.) In Fig. 3.4(f,) the I_{ds}-V_{ds} characteristics measured in the p- channel also shows linear behavior and exhibit similar level of on currents as previously observed for the n-channel at IL gate =6 V. This finding indicates for the low resistance contacts can be achieved by this graphene contact gated with applying IL-gate. It is capable of being image that a small SB still appear in our graphene-contacted WSe_2 devices, the resistance of the contact is drastically reduced by the combined effect of SB height reduction and width narrowing when applying IL gate. The contact resistance of the device was estimated from the I-V characteristics at high V_{bg} and high V_{ILg} of a short channel where the separation is ≈200 nm which is further determined in detail in section 3.4.4. The contact resistance has been extracted shows less than 2kΩ·μm, which is lower than the reported contact resistance of 7×10^5 Ω.μm for Ti and 6.5×10^3 Ω.μm for Ag electrodes in few layer WSe_2 FETs.[77]

Figures 3.5 (a) and 3.5 (b) show the p- and n- channel transfer characteristics of the same device which characterized in Figure 3.4, the conductivity is defined by the equation of $\sigma=I_{ds}/V_{ds}\times L/W$, where L is the length and W the width of the channel where is passivated by the h-BN at the WSe_2 channel with the temperature between 77 and 160 K. It is clear to see that conductivity increases with decreasing temperature for electron and hole channels at high positive and high negative back gate voltages. Interestingly, we observed with increasing hole density, a crossover of metallic to insulating region. Where for the insulating region, the

conductivity increases with increasing temperature, and for the metallic regime, the conductivity decreases with temperature.

We also observed the crossover occurs at the critical quantum conductivity of e^2/h, consistent with the observed metal-insulator transition (MIT) in monolayer, bilayer and multilayer MoS_2 as well as theoretical expectations for 2D semiconductors.[85,88,108] However, the MIT we observed in our WSe_2 device presented at a lower carrier density of $\approx 1\times10^{12}$ cm^2 where in MoS_2 , the carrier density $\approx 1\times10^{13}$ cm^2, may be attributed to the lower level of impurity states inside the band gap of our h-BN passivated WSe_2 devices than in previously reported MoS_2 devices.[85] Here, we use the model of $C_{bg} \times (V_{MIT} - V_{th})/e$ to determine the critical carrier density for the MIT, where V_{MIT} is the back gate voltage of the MIT and V_{th} is the threshold voltage. For the electron channel, this MIT is considerably suppressed, as showing in Figure 3.5(a.) And since our WSe_2 single crystals are slightly p-doped, the impurity states in the band gap are presented to be close to the valence band edge. As results in the conduction band should be more affected by the disorder than the valence band. Furthermore, to confirm there are more impurity states in the gap near the valence band edge than the conduction band edge, we observed that the threshold voltage for the n channel is close to $V_{bg} = 0$ V, where p channel is close to -20 V. As the chemical potential of the WSe_2 channel is shifted toward the valence band with applying back gate, it crosses localized band tail states before reaching the valence band, resulting in a non-negligible threshold voltage. On the other hand, the significant lower density of impurity states near the conduction band edge allows the electron channel to be shifted on much more quickly by a gate voltage, resulting in the threshold voltage can be significantly reduced.[109] Also the observation of a MIT in the hole channel is unlikely a hysteretic effect due to the small hysteresis in the transfer characteristics showing in Figures 3.4(b) and 3.4(c.) It is to be further

investigate that to rule out the absence of a MIT for hole and electron channels is due to the hysteresis influencing in presence due to nearly identical behavior of the transfer characteristic curve from dual sweep measurement at temperature between 77K and 160K.[16]

In Fig. 3.5(c,) Field-effect mobility is extracted from the V_{bg} dependence of σ using the expression $\mu = (1/C_{bg}) \times (d\sigma/ dV_{bg})$ in the linear region of the σ vs V_{bg} curves, where C_{bg} is the back-gate capacitance per unit area. Based on a simple parallel-plate capacitor model, C_{bg} is determined to be 1.2×10^{-8} F cm^{-2} for 290 nm SiO_2 ($C_{bg} = 3.9 \times \varepsilon_0/290$ nm). We obtain the temperature dependence of the hole and electron field effect mobility, extracted from the linear region of the metallic state at the high back gate voltage in transfer characteristic, where -45 V < V_{bg} < -35 V for the hole channel and 10 V < V_{bg} < 20 V for the electron channel. The mobility of electron channel increases from 196 $cm^2V^{-1}s^{-1}$ to about 330 $cm^2V^{-1}s^{-1}$ as the temperature decreases from 160 K to 77 K, where the hole channel increases similarly from 204 $cm^2V^{-1}s^{-1}$ to about 270 $cm^2V^{-1}s^{-1}$. The high mobility values observed here are comparable to the highest mobility values reported in thin film WSe_2 FETs.[75,77,79] At the high back gate region, the mobility increases with decreasing temperature also strongly suggests that its intrinsic channel properties has been observed which are dominated by phonon scattering. It is important that by using ultra-flat and ultraclean h-BN passivation layer to the channel for minimizing the presence of interface trap states is critical for the achievement of high mobility along with low threshold voltages. The evidence is also showing in chapter 3.3.2 the lower mobility and higher threshold voltages was observed in WSe_2 devices, where the channel was covered by a 50 nm thick Al_2O_3 layer with the E-beam deposition. In comparison of the performance of device with the difference geometry 3.3.1 and 3.3.2 to 3.3.3., Where first, the transfer characteristics of the bear WSe_2 device is qualitatively consistent with that of the h-BN passivated devices in the section

3.3.3, and The mobility observed in the bear sample is also smaller in comparison to the h-BN passivated device discussed in section 3.3.3 which further indicates that channel passivation with ultraclean h-BN is critical for studying intrinsic channel properties.

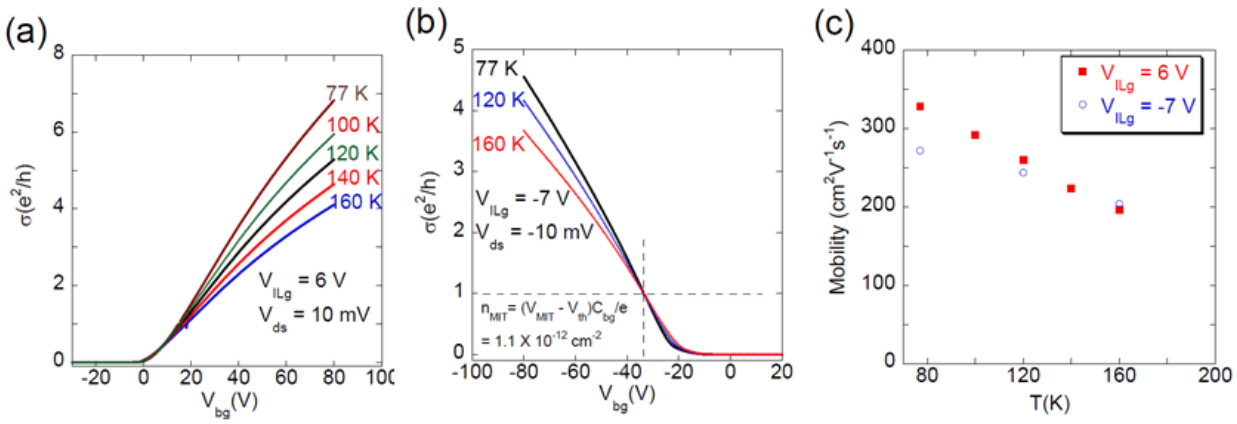


Figure 3.5 The temperature-dependent two-terminal transfer characteristic as a function of the back gate voltage, extracted from the same WSe_2 device presented in figure 3.4, with applying at (a) V_{ILg} = 6 V for n-channel and (b) V_{ILg} = -7 V for p-channel. (c) Temperature dependent twe terminal field-effect mobility in the WSe_2 device extracted from two-terminal conductivity measurements as a function of the back-gate voltage at V_{ILg} = 6 V and V_{ILg} = -7 V.

Furthermore, it is clear that the threshold voltage for both the hole and electron channels in the Al_2O_3 passivated device is much larger than in the h-BN passivated device shown in comparison in Fig. 3.3 and 3.5. Figure 3.3(c) shows that the field-effect mobility is also much lower in the Al_2O_3 passivated device than in the h-BN passivated device, which can be attributed to additional charge traps and interface roughness introduced by Al_2O_3.

The temperature dependence electrical measurements of WSe_2 FETs with low-resistance graphene contacts reveal presented the temperature decreases from 160 K to 77 K, the extrinsic field-effect mobility increases from ≈196 $cm^2V^{-1}s^{-1}$ to ≈330 $cm^2V^{-1}s^{-1}$ for the electron channel and from ≈204 $cm^2V^{-1}s^{-1}$ to ≈270 $cm^2V^{-1}s^{-1}$ for the hole channel. These mobility values are comparable to the highest electron and hole mobility reported on thin film WSe_2 FETs as well as bulk WSe_2[75,77,79,102] which is the indication of our graphene-contacted few-layer WSe_2 devices

approach the intrinsic phonon-limited mobility for both electrons and holes. The most significant property of this study is that highly tuned (doped) graphene contact is an excellent contact electrode material for high-performance hole channel and electron channel TMDS FETs. The different functionalities of highly n-doped and highly p-doped graphene electrodes offer a promising possibility to fabricate complementary digital circuits on a single TMDS thin film.

3.3.4 Contact resistance of graphene contacted device

Figure 3.6a shows the output characteristics of a short-channel device (channel length L ≈ 200 nm) with IL-gated graphene contacts. The ON-state resistance of the device, measured at a high IL-gate voltage and a high back-gate voltage in the linear low drain-source voltage region between electrodes labeled 3L and 4 in Fig. 3.6 (c,) is determined to be 5 kΩ. This resistance consists of the metal/graphene contact resistance, the graphene electrode sheet resistance, the WSe_2 channel resistance, and the graphene to WSe_2 contact resistance. To isolate the contact resistance of the graphene-WSe_2 junctions, we also measured the resistance of a graphene sheet and the metal-graphene contacts separately. As shown in Fig. 3.6(b,) the total resistance measured between electrodes 2L and 2R in Fig. 3.6(c) is 2.2 kΩ. As suggested by the device layout in Figure 3.6(c), i) the total resistance between electrodes 2L and 2R should be comparable to that between electrodes 3L and 3R; and ii) the metal-graphene contact resistance and graphene electrode sheet resistance are likely much smaller for electrode 4 than electrode 3L, given the much longer metal-graphene contact length and smaller L/W ratio for electrode 4 than 3L. Therefore, the maximum contact resistance of a graphene/WSe_2 junction is estimated to be $R_c = (R_{ON}-R_{G\text{-}ele})/2 = (5\ k\Omega - 2.2\ k\Omega/2)/2 \approx 2\ k\Omega$. Since the width of this particular WSe_2 sample is 1.0 μm, the normalized contact resistance of the graphene/WSe_2 junction is less than 2 kΩ·μm.

In order to quantitatively study the graphene/WSe_2 junction and the intrinsic WSe_2 channel properties, it is important to minimize the graphene sheet resistance and graphene to metal contact resistance. Low sheet resistance of ~100 Ω/sq has been obtained in monolayer graphene that had been electrostatically doped up to 3×10^{13} cm^{-2} by ferroelectric dipoles[53]. Low metal-graphene contact resistance of the order of 10^2 Ω·μm has been routinely achieved by selecting proper contact metal[54]. The graphene sheet resistance and the graphene-metal contact resistance can be further minimized (i) by shaping the graphene electrodes in such a way that the metal/graphene contact area is much larger than that of the graphene/WSe_2 interface, and (ii) by electrostatically doping on graphene electrodes up to very high carrier concentration of ~ 10^{14} cm^{-2} using an IL.

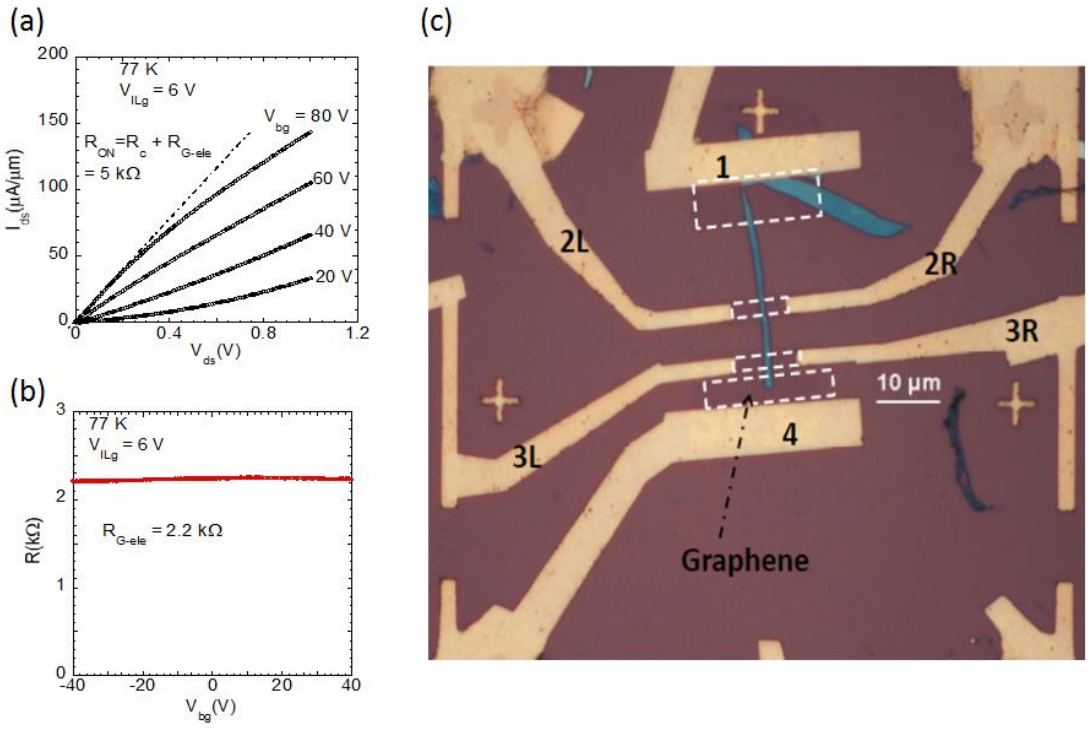


Figure 3.6 (a) Output characteristics of a short channel (L≈ 200 nm) WSe_2 device shown between electrodes 3L/3R and 4, depicted in panel (c), at a high IL-gate voltage of 6 V. (b) The resistance of a graphene FET device between electrodes 2L and 2R, depicted in panel (c), at a high IL-gate voltage of 6 V. (c) Optical micrograph of a 8 nm think WSe_2 sample contacted by

graphene electrodes in the area highlighted by the white dashed lines. The channel length between electrodes 3L/3R and 4 is about 200 nm.

3.3.5 Transfer characteristic with double-sweep measurement

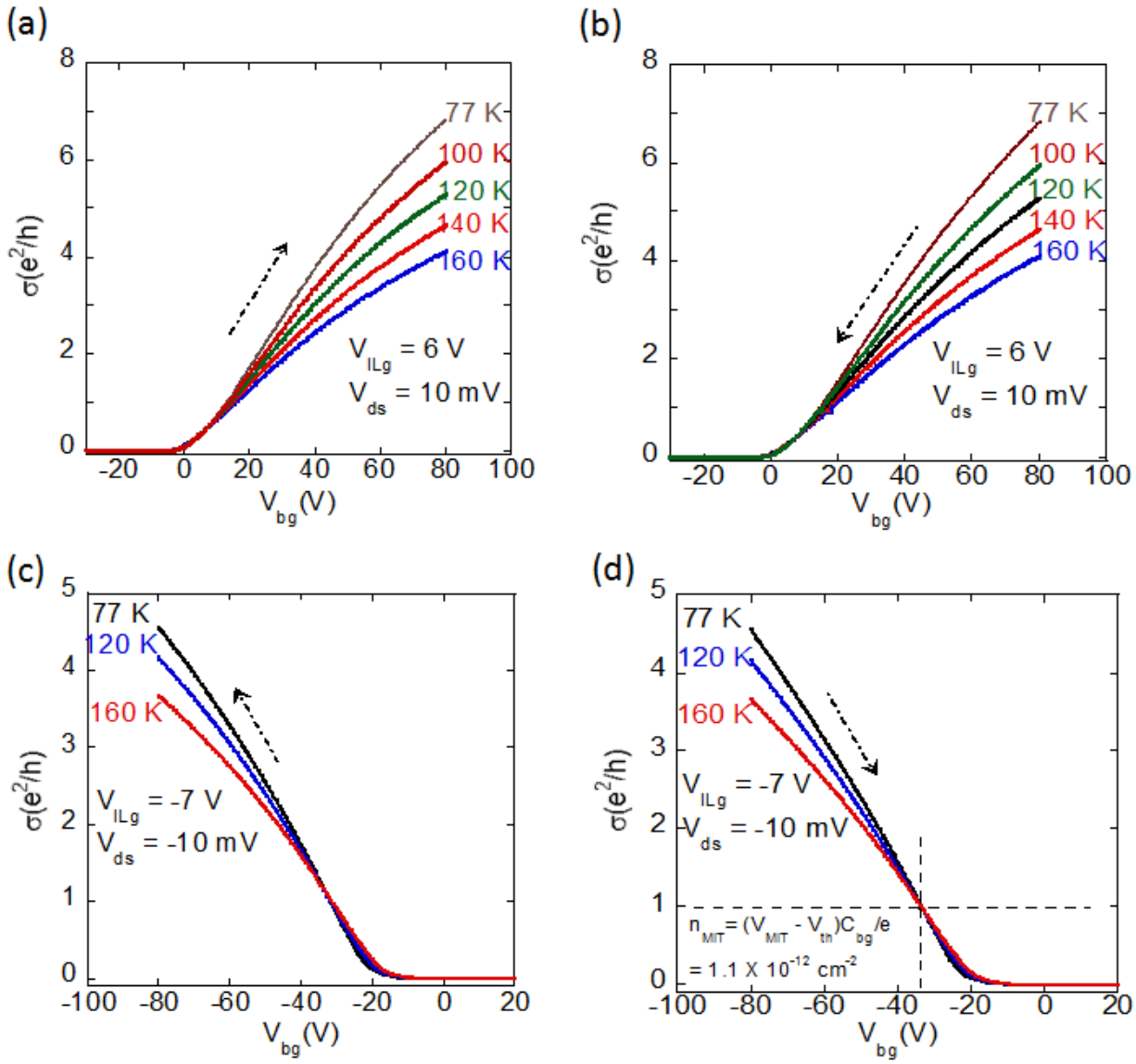


Figure 3.7 Temperature dependent two-terminal conductivity as a function of the gate voltage for the WSe_2 device shown in figure 3.4 with dual-gate sweep directions, obtained after it was cooled down from 230 K at the IL gate voltages. (a,) (b) V_{ILg} = 6 V and (c,) (d) V_{ILg} = -7 V. The direction of the gate sweep is indicated by the arrow in the figure.

3.3.6 Ionic Liquid gating effect on graphene FET

We have previously shown that the IL deposited on our FET devices is unlikely to change the back-gate capacitance of the device below the freezing temperature of the IL.[2] To further rule out the possibility of the IL droplet changing the back-gate capacitance in our graphene-contacted WSe_2 devices even below the freezing temperature of the IL, we have measured the transfer characteristics of a graphene FET fabricated on WSe_2 before and after depositing the IL. Figure 3.8 shows that the overall shape of the transfer curve of a graphene FET on the WSe_2 substrate does not change after depositing IL with the exception of the Dirac point, which is slightly shifted due to the small amount of IL-induced doping. This further confirms that the deposition of the IL on our devices does not change the back-gate capacitance.

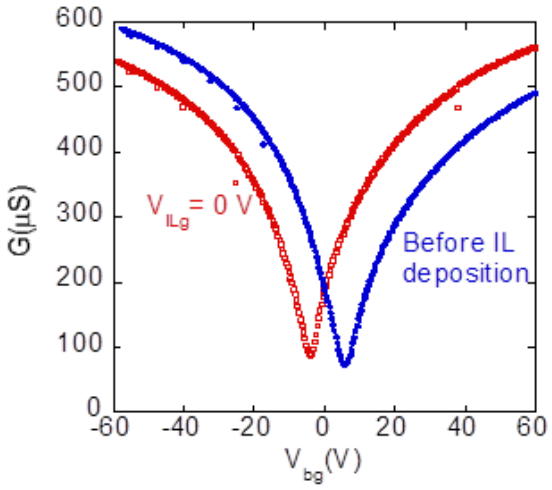


Figure 3.8 The comparison to the transfer characteristics of a graphene FET device on WSe_2 substrate as a function of the back-gate voltage before and after deposition of the IL with IL gate =0V.

In addition to TMDs FET devices, we have also presented Schottky diode operations in our WSe_2 devices by applying IL gate voltages to the two graphene to WSe_2 contacts asymmetrically.[111] Our Schottky diode device displays a significant rectifying behavior and a diode ideality factor of ~1.3, indicate the high quality of the graphene/WSe_2 interface.

3.3.7 Performance of Schottky Diode

To further characterize the interface quality between graphene to WSe_2, Schottky diode device is presented that is dominated by a single graphene/WSe_2 SB. The Schottky diode behavior in this device was presented by applying asymmetric IL gate voltage to create one high-resistance contact and low-resistance contact to the other.[111] Figure 3.9(a) shows the Schottky diode characteristics on an n-type graphene to WSe_2 SB junction measured with the back gate voltages of V_{bg} = 20 V and 30 V. The positive back-gate voltages were used to turn on the electron channel so high-resistance graphene/WSe_2 SB junction was dominated in the entire device. Resulting in the ideality factor of ≈ 1.3 of the device. Where the diode was obtained in the forward region at low bias voltages. The ideality factor is close to 1.0 also indicated the quality of interface is close to ideal interface cleanness in this device.[92] Moreover, the usage of the SB diode can be used to extract the SB height from the temperature dependence of the diode characteristics, where it excludes the complications from back-to-back SB contacts for the most TMDs FET devices.

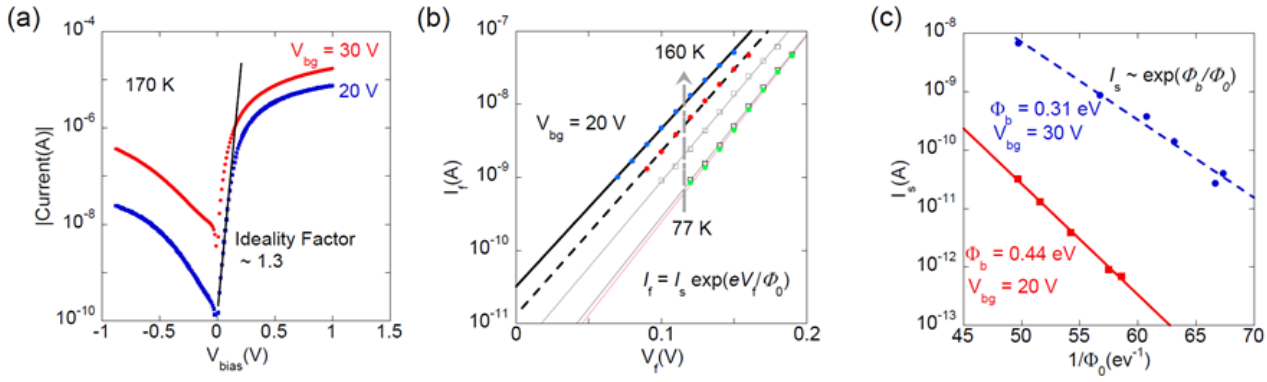


Figure 3.9 (a) The Schottky diode behavior is observed in Semi-Log Plot of I-V output characteristics of a graphene/WSe_2 Schottky barrier (SB) at fixed back-gate voltages of V_{bg} = 20 V and 30 V, (b) Forward-bias of I_f-V_f characteristics dominated by a single graphene/WSe_2 SB junction with temperature in between 77 K and 160 K. (c) The plot of saturation current I_s as a function of the inverse characteristic energy Φ_0 extracted from (b). The SB height is determined by using the exponential fitting function in the insert of the figure.

At the contact region, the WSe_2 with the graphene drain and source electrodes is mostly electrostatically doped by the back gate voltage, where it has been applied to turn on the channel, as well as by the IL gate voltage. In which case, the current injection from the graphene/WSe_2 SB junction is thought not to be dominated by thermionic emission but thermally assisted tunneling. Thus, in our SB diode, the commonly used thermal activation method is expected to underestimate the SB height. In order to obtain a better estimate of SB height at the junction of this device, we have obtained a model that considers the thermally-assisted tunneling current to highly doped semiconductors through the SB.[112,113] It is showing in Figure 3.9(b) that forward I-V characteristics at the exponential region, where appears to be linear in the semi-logarithmic plot, measured at temperatures in between 160K to 77K for one thermal cycle to avoid possible thermal hysteresis effects. Resulting in the data which are well fitted by the equation of $I_f = I_s \exp(eV_f/\Phi_0)$, where I_s is the saturation current at zero forward voltage ($V_f = 0$ V,) and Φ_0 is a characteristic energy, for both are strongly temperature dependent. Furthermore, the saturation current I_s also depends on exponentially on $1/\Phi_0$. From Figure 3.9(c), where the $V_{bg} = 20$ V, from the semi-logarithmic plot of I_s as a function of $1/\Phi_0$ with usage of I_s and Φ_0 values to obtain from fitting our data with different temperatures, is shown in Figure 3.9(b) with $V_{bg} = 30$ V. To fit the data for the saturation current I_s in Figure 3.9(c) by the expression of $I_s \sim \exp(\Phi_b/\Phi_0)$, we obtain Φ_b=0.44 eV as a SB height of the graphene/WSe_2 junction at V_{bg}= 20 V and the lower value Φ_b=0.31 eV at V_{bg}=30 V. Note that the difference between the graphene work function and the conduction band minimum in WSe_2.[71] is also agree with the reduction of SB height at increasing back gate voltage. It can also be attributed to the back gate tuning of the graphene work function where the relatively low carrier density in the WSe_2 layer is not enough to screen out the electric field applying from back gate voltage. With the absence of Fermi level pinning

effect and electric field screening, tunability of the graphene work function for the maximum is estimated to be up to 0.2 eV which is close to the charge neutrality point of a graphene monolayer for a back-gate voltage range of 10 V in our device. The work function of the graphene contacts is also insensitively to the back gate voltage with mainly determined by the IL gate at high V_{ILg} values, due to the extremely high carrier density in graphene and the much larger IL gate capacitance. When back gate voltage changes by 10 V, that the graphene work function changes by about 70% of the theoretical limit which also indicates that Fermi level pinning is nearly absent in our graphene to WSe_2 junctions so that graphene is close to its charge neutrality point, given that the gate electric field is likely partially screened by the thin WSe_2 layer between graphene and the back gate.

Low-resistance contacts devices fabricated in my study with utilizing the highly doping graphene at the graphene to WSe_2 region by using large IL-gate voltages which enable us to study the intrinsic properties of both the hole and electron channels in TMDS on the same device investigate for the first time.

In summary, we have presented to fabricate both electron channel and hole channel WSe_2 FETs with ultra clean hexagonal boron nitride as a protection layer to encapsulate the channels and graphene as a contact with ionic-liquid-gating resulting in the intrinsic transport properties of the channel. Including a MIT (metal-insulator transition) at a characteristic conductivity nearly the quantum conductance (e^2/h), and the high device performance of ON/OFF ratio more than 10^7 at 170 K along with the electron and hole mobility exceeding $\mu \approx 200$ $cm^2V^{-1}s^{-1}$ at 160 K. With decreasing temperature down to 77 K, the 2 probe field effect mobility of electron increases to nearly 330 $cm^2V^{-1}s^{-1}$and the holes of exceeding 270 $cm^2V^{-1}s^{-1}$. As the result, the intrinsic phonon limited channel property was observed for both electron and hole side due to the drastic

Schottky barriers reduction in between the channel and the graphene contact electrodes with usage of IL gating. Also with the achievement it allowed us to elucidate the process by using single sided graphene to WSe_2 Schottky diode device. The result of the Low-resistance contact achieved by utilizing the IL-gated graphene devices, gives the wide range of 2D semiconductor application.

With this method of the low resistance contact was enabled by using the work function tunability of graphene as the device contacted along with the usage of IL gating lead us to further considering more opportunities for the TMDS electronic device applications. However, this method is still not compatible for the practical applications which need more permanent and air-stable contacts. Therefore the next strategy of this study is further discussed in chapter 4.

3.3.8 Other doping method: BV and F4TCNQ

Other than the IL gated graphene contacted WSe_2 FETs, we have also achieved the ohmic contact by using BV and F4-TCNQ doping method on graphene since the IL gating does not allow to have access for the transport measurement above IL frozen point(200K), which the applying method is showing in the previous section of 2.4.3.

BV and F4-TCNQ is expected as an air stable doping substance solution of electron and hole doping respectively. Here we first test out on the graphene FETs device and it shows a great doping level on graphene showing in Fig. 3.10. The comparison of the performance of the two-terminal graphene contacted WSe_2 device with applying VB and TCNQ doping at the room temperature shows in the Fig. 3.11. Transfer Characteristics show good device performance with an on/off ratio of 7 orders of magnitude with back gate voltage =1V. The inset of Fig. 3.11 shows that linearity of I-V characteristics indicates near Ohmic contact due to the reduction of the Schottky barrier by applying air stable surface charge transfer doping method on graphene

contacted device. With the promising result we further investigate the transport properties with the 4 terminal WSe_2 device, showing in the Fig. 3.12.

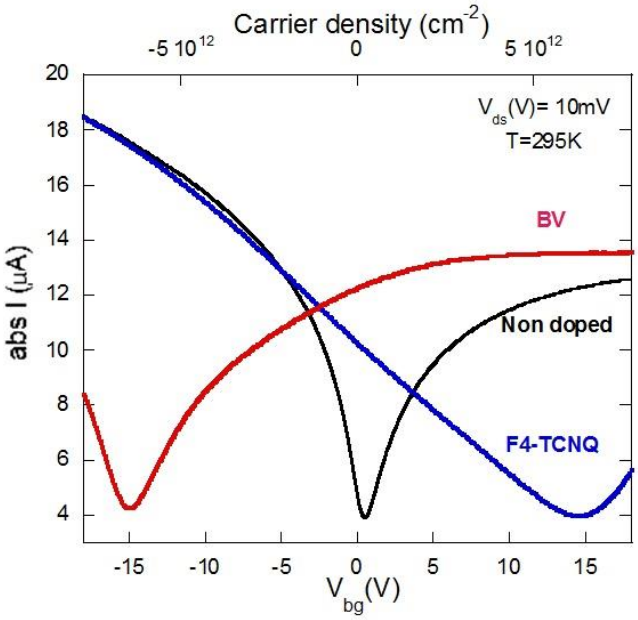


Figure 3.10 The doping method on the same graphene FET that is on the side of the same WSe_2 FETs, as the result show the Dirac point of graphene shifted significantly to the right (with negative back gate voltage) and right (with positive gate voltage) when apply BV (red cove) and F4-TCNQ(blue) respectively. Notice that the Dirac point is near zero back voltage without applying any doping substance on the graphene.

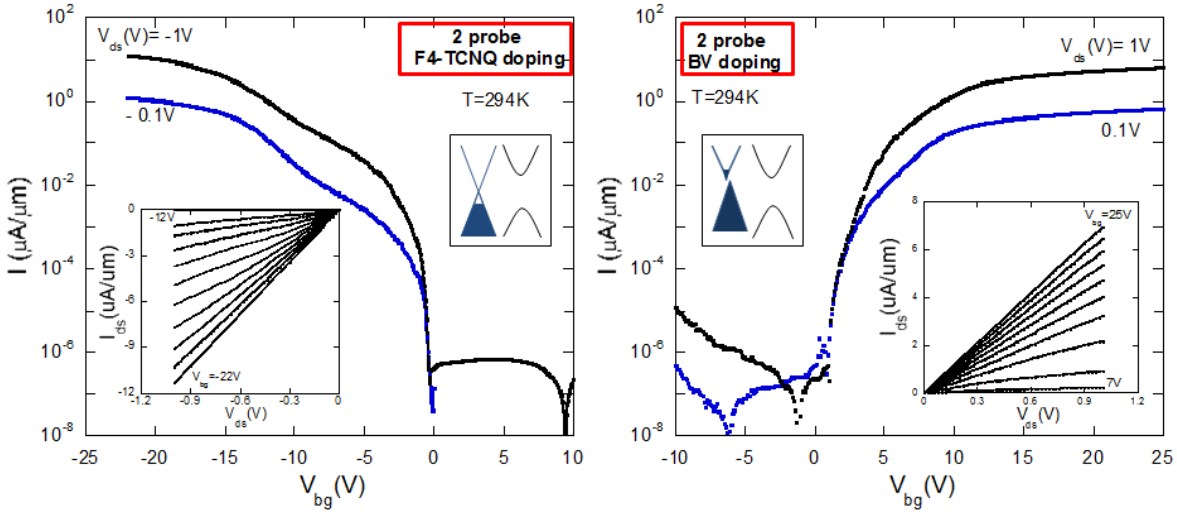


Figure 3.11 The room temperature of the very same device with applying BV (left) and F4-TCNQ (right) on the graphene contacted device with the drain bias of -1V (black) and -100mV (blue.) The inset of I-V output characteristic shows highly linear behavior for both cases indicates the significant SB has been reduced with the doping method.

Figure 3.12 demonstrates the significant intrinsic channel behavior for both electron and hole channel, with the high 4 terminal field effect mobility. Also note that result is showing hole mobility is higher than electron mobility, which can be attributed to the smaller effective mass of holes compared to electrons in WSe_2, also the gamma value for electron side is similar to the gamma of MoS_2 reported previously indicates the minimum of charge impurity scattering of the device Nevertheless, the gamma for hole is around 1.5 may suggest the possibly different scattering mechanisms for holes and holes in WSe_2.

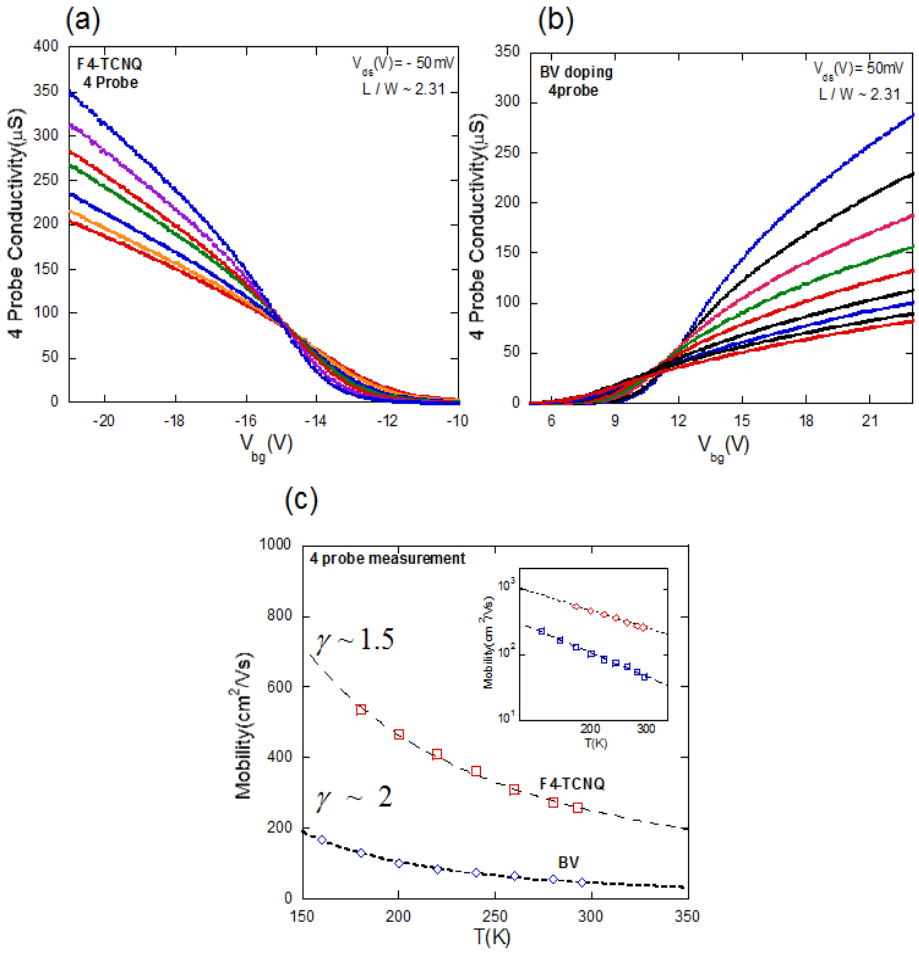


Figure 3.12 Four terminal graphene contacted device with BV, F4-TCNQ doping method which enabled the low resistance contact of the device from room temperature down to low temperature. (a), (b) shows the transfer characteristic with the observation of intrinsic phono limited behavior of the channel. (c) Shows the 4-terminal field effect mobility as a function of temperature with the inset of semi log plot.

CHAPTER 4 NEW APPROACH TO LOW-RESISTANCE 2D/2D OHMIC CONTACTS OF HIGH-PERFORMANCE WSe_2 AND MoS_2 TRANSISTORS

With the success and the promising results[1] from the previous method in chapter 3, it interests us to further study the possibility of achieving more universal method for low resistance contact, high performance TMDs electronic devices. Therefore, in this chapter, we introduce a new strategy[2] by using vdW assembly of substitutionally doped TMDs as drain/source contacts and TMDs with no intentional doping as channel materials for a variety of TMDs, which we call "2D/2D contacts" is formed. Our few-layer WSe_2 field-effect transistors (FETs) with degenerately p-doped WSe_2 drain/source contacts exhibit low contact resistances of ~ 0.3 kΩ μm, high on/off ratios up to > 10^9, high drive currents exceeding 320 μA $μm^{-1}$. These unique characteristics are combined with a two-terminal field-effect hole mobility $μ_{FE} ≈ 2×10^2$ $cm^2 V^{-1} s^{-1}$ at room temperature, which increases to $>2×10^3$ $cm^2 V^{-1} s^{-1}$ at cryogenic temperatures. We also observe a similar performance in MoS_2 and $MoSe_2$ FETs with degenerately p-doped MoS_2 drain and source contacts. The 2D/2D low-resistance ohmic contacts presented here demonstrates a new device paradigm that overcomes a significant challenge in the performance of TMDs and other 2D materials as the channel materials in post-silicon electronics.

4.1 Background

Fabricating high-performance transistors of TMDs including WSe_2, MoS_2, and $MoSe_2$ has been a major challenge in 2D electronics,[114,115] and in most cases the main limiting factor to the performance of current metal-contacted TMDs is the presence of a significant Schottky barrier at the contact region of the electronic devices. Various strategies have been reported to reduce the contact barrier, for instance, surface and substitutional doping,[116-120] phase-engineering,[121,122] and the use of graphene contacts.[1,123,124] However, these methods are still deficient in their

insufficient air or thermal stability, limited spatial definition of the contact regions, or do not offer true ohmic contact behavior. The nature of TMDs facilitates cleavage and formation of ultrathin layers, which are considered as suitable semiconducting counterparts to semi-metallic graphene and may lead to application of flexible electronics and optoelectronics.[124,125-127] These systems have showed many graphene-like properties which include relatively high carrier mobility, mechanical flexibility, chemical and thermal stability, and moreover it offers the significant advantage of a substantial band gap that is essential for digital electronics.[128] However, TMDs tend to form a substantial Schottky/tunneling barrier with most metals commonly applied for fabricating electrical contacts.[116,129] Under certain chosen contact metals with a proper work functions, the barrier height has turned out to be drastically reduced by Fermi level pinning.[130-132] In silicon-based electronics, selective ion implantation of drain/source regions below metal electrodes enables low-resistance ohmic contacts, and with this method, the contact barrier width between the metal electrodes and degenerately doped source and drain regions is significantly reduced. Unfortunately, the ultrathin body of monolayer and few-layer TMDs inhibits effective doping by ion implantation, hence, various alternative doping methods such as surface charge transfer doing[116-118,133] and substitutional doping[6,7] have been utilized to reduce the Schottky barrier width and result into decrease of the contact resistance of TMD devices; however, most of these doping methods yield devices with a poor air, thermal or long-term stability. In this aspect, substitutional doping appears to be a suitable alternative, since dopants secured by covalent bonding (e.g. Nb doped MoS_2) during the material synthesis yield devices with excellent air and thermal stability.[120] Conventional substitutional doping during synthesis poses the limitation of the inability to form a spatially abrupt doping profile, which

defines the drain, the channel and the source regions that is needed for high-performance electronics.

4.2 The New strategy to 2D/2D vertical junctions of Contact Engineer

In this section, we present a new strategy that utilizes 2D/2D vertical junctions to engineer low-resistance ohmic contacts, which turn TMDs including WSe_2, MoS_2 and $MoSe_2$ into high-performance transistors. 2D/2D junctions with atomically sharp interfaces can be created by vdW assembly of 2D crystals without the constraints of atomic commensurability. The working principle, device fabrication, and the device performance will be addressed in great detail in following sections.[134,135]

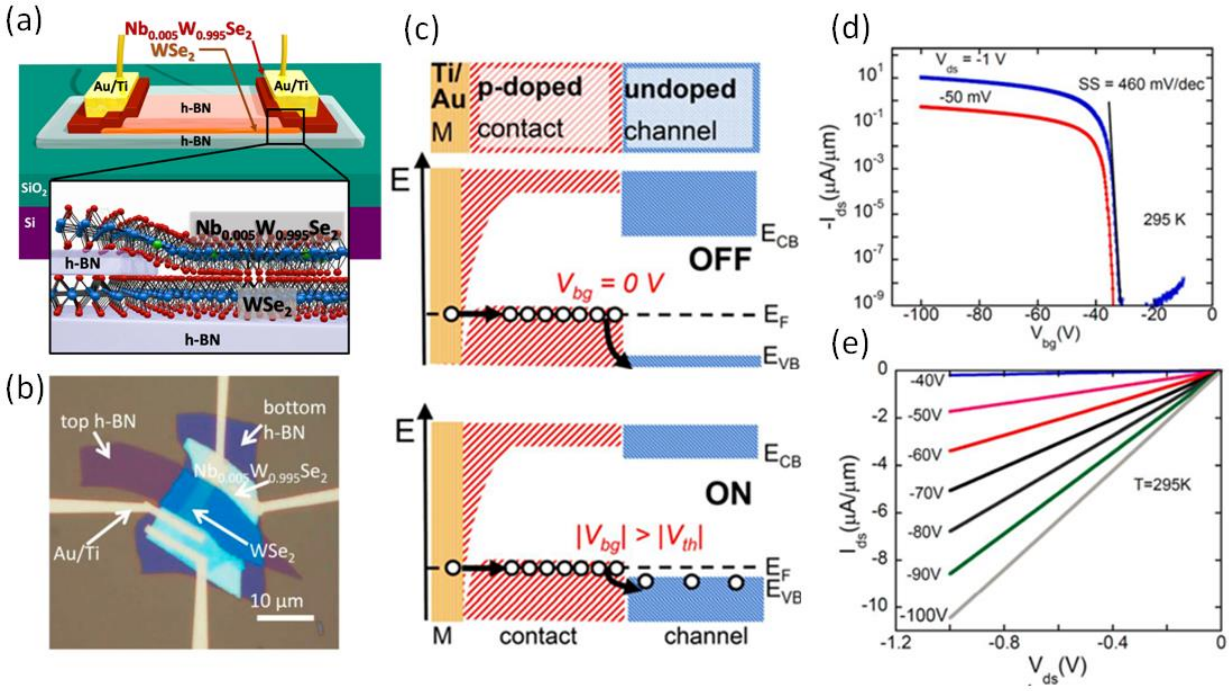


Figure 4.1 Shows high-performance WSe_2 FET with 2D/2D contacts. (a) The WSe_2 FET side view with degenerately p-doped WSe_2 ($Nb_{0.005}W_{0.995}Se_2$) contacts. (b) Optical micrograph of the device. The channel region is showing encapsulated by h-BN from the top and the bottom. (c) Band diagram indicates in the off- and the on-state of the FET with 2D/2D contacts. Holes are injected from a metal into a highly p-doped WSe_2 contact layer through a highly transparent metal to contact interface. Hole injection from the drain/source contact layer across the 2D/2D interface into the undoped WSe_2 channel is tuned by the gate voltage V_{bg}. (d) Modulation range of the source-drain current I_{ds} by the back-gate voltage V_{bg} leads an on/off ratio of up to $>10^9$ at

room temperature in a WSe_2 FET with a 10.8 μm long and a 3.0 μm wide channel. (e) Linearity of the I_{ds}-V_{ds} characteristics shows highly ohmic behavior for a wide range of back-gate voltages.

4.2.1 Device preparation and methods

Figure 4.1(a,) (b) present a schematic diagram and optical micrograph of a WSe_2 FET device composed of degenerately p-doped WSe_2 ($Nb_{0.005}W_{0.995}Se_2$) 2D drain/source electrodes in contact with a 2D WSe_2 channel with no intentional doping. Fabrication of devices containing TMDs such as WSe_2 involved artificially stacking of mechanically exfoliated flakes of degenerately p-doped TMDs which is considered as electrodes, on top of an undoped TMD channel material with a dry transfer method.[1] Subsequently, metal electrodes were formed by deposition on top of the degenerately doped TMD contacts and are consist of 10 nm Ti / 40 nm Au; the growth condition and detail were expressed in detail in chapter 2.1.3. To preserve its intrinsic electrical properties, the TMD channel material was encapsulated in hexagonal boron nitride (hBN).[1,136] Similar to degenerately doped silicon in Si electronics, degenerately doped TMDs also form low-resistance ohmic contacts with top metal electrodes where the device fabrication is been addressed in chapter2. Consequently, the total contact resistance of our devices is primarily determined by the resistance of the 2D/2D junctions between the degenerately doped TMDs, acting as source/drain electrodes, and the undoped TMD channel material. All of the crystals of degenerately doped and undoped TMDs used in this work were synthesized by chemical vapor transport except for undoped MoS_2 crystals, which were purchased from SPI Supplies. Optical microscopy and atomic microscopy (AFM) with noncontact mode of Park-Systems XE-70 were used to identify and characterize thin $MoSe_2$ flakes.

TMDs devices with 2D/2D contacts were made by conventional exfoliation of degenerately doped and undoped ultrathin TMDs crystals on separate PDMS stamps. The degenerately doped

TMDs flakes formed the drain and source electrodes, were then manually stacked using a dry transfer method (chapter2) on top of undoped TMDs flakes that formed the channel. Electrical properties of the devices were measured by a Keithley 4200 semiconductor parameter analyzer in a Lakeshore Cryogenic probe station under high vacuum (1×10^{-6} Torr) or in a Quantum Design PPMS.

4.3 Homojunction device

4.3.1 Working principle

The band diagram and working principle of the 2D/2D contacts are demonstrated in Fig. 4.1(c.) Different carrier densities resulted into differences in work function between the undoped channel and the highly doped drain/source and it creates a band offset across the 2D/2D interface at the contact region of device. At the junction interface of conventional 3D semiconductor junctions, the band offset is usually well-defined by the covalent bonds. The band offset can be electrostatically tuned by a back-gate voltage,[23,24] since the inter-layer interaction in 2D TMDs and their junctions is much weaker. Hence, we used the advantage of this unique property of 2D/2D junctions to form spatially sharp, tunable, true ohmic contacts of TMDs electronic devices.

The top panel of Fig. 4.1(c), shows there are no free carriers in the channel in the off-state with no applying the back-gate voltage (V_{bg}=0 V). Increasing the negative back-gate voltage shifts up all bands in the channel material up, in contrast to the bands in the highly doped electrodes remain unaffected. As illustrated in the bottom panel of Fig. 4.1(c), modified band alignment thus introduces holes in the channel material. Contact barrier at the interface essentially vanishes and low-resistance contact is achieved in the on-state when the gate voltages exceed the threshold ($V_{bg}<V_{th}$.)

4.3.2 Device Performance of p-Wse2

Figure 4.1(d,) (e) show the transfer and output characteristics under room-temperature of a 5-layer WSe_2 FET that is encapsulated in hBN. This ~3.5 nm thick device is contacted by degenerately p-doped WSe_2 ($Nb_{0.005}W_{0.995}Se_2$) and measured by using a Si back gate. Transfer characteristics shows clear p-type behavior with an exceptionally high on/off ratio $>10^9$ at V_{ds} = -1 V and a subthreshold swing of ~460 mV/dec, which can be further reduced to the near-ideal value of ~63 mV/dec by using a top gate with hBN gate dielectric where is expressed in detail in section 4.3.6. The significant enhancement of the on-current that is enabled by the low-resistance 2D/2D contacts is one of the reasons that may results into the high on/off ratio. As shown in Fig. 4.1(e,) the on-state drain current is linear at all back-gate voltages, indicating ohmic behavior. Low-resistance 2D/2D contacts also enable us to evaluate the intrinsic properties of the channel. Figure 4.2(a) indicates the temperature-dependent two-terminal conductivity of another WSe_2 device that is 3.5 nm thick, ≈14.8 μm long, ≈4.7 μm wide, and passivated by h-BN**.** The two-terminal conductivity is defined by $\sigma=I_{ds}/V_{ds}\times L/W$, where L is the length and W the width of the channel. With the increasing of hole concentration, the WSe_2 device displays a crossover from an insulating regime to a metallic regime, where the conductivity increases with increasing temperature indicates insulating regime, while the metallic regime shows conductivity decreases with temperature. From the inset of Fig. 4.2(a,) at a critical conductivity of ~e^2/h the metal-insulator-transition (MIT) can be more clearly seen in the corresponding temperature-dependent conductivity that consistent with the MIT observed previously in MoS_2, $MoSe_2$ and WSe_2.[1,137,138] The MIT observed here is unlikely a hysteretic effect, since the duel sweeping measurement shows the measurement with opposite gate-sweeping directions is mainly overlapped.

As seen in the inset of Fig. 4.2(c,) the output characteristics of the device remain linear down to 5 K, confirming a true ohmic contact at the 2D/2D interface which is free from a Schottky barrier. Consequently, at V_{bg} = -80 V, the on-state conductivity increases monotonically by a factor of ~6 as the temperature decreases from 300 K to 5 K. The temperature-dependent field-effect hole mobility of the WSe_2 device is shown in Fig. 4.2(c.) The field effect mobility can be extracted from the linear region of the conductivity curves in the metallic state at -80 V < V_{bg} < -50 V by the expression of $\mu_{FE} = (1/C_{bg}) \times (d\sigma/dV_{bg})$, where C_{bg} is the back-gate capacitance based on the parallel plate model. The back-gate capacitance can also be determined from Hall measurement on a similarly hBN-encapsulated WSe_2 Hall bar device which is consistent with its geometric capacitance in section 4.3.8.

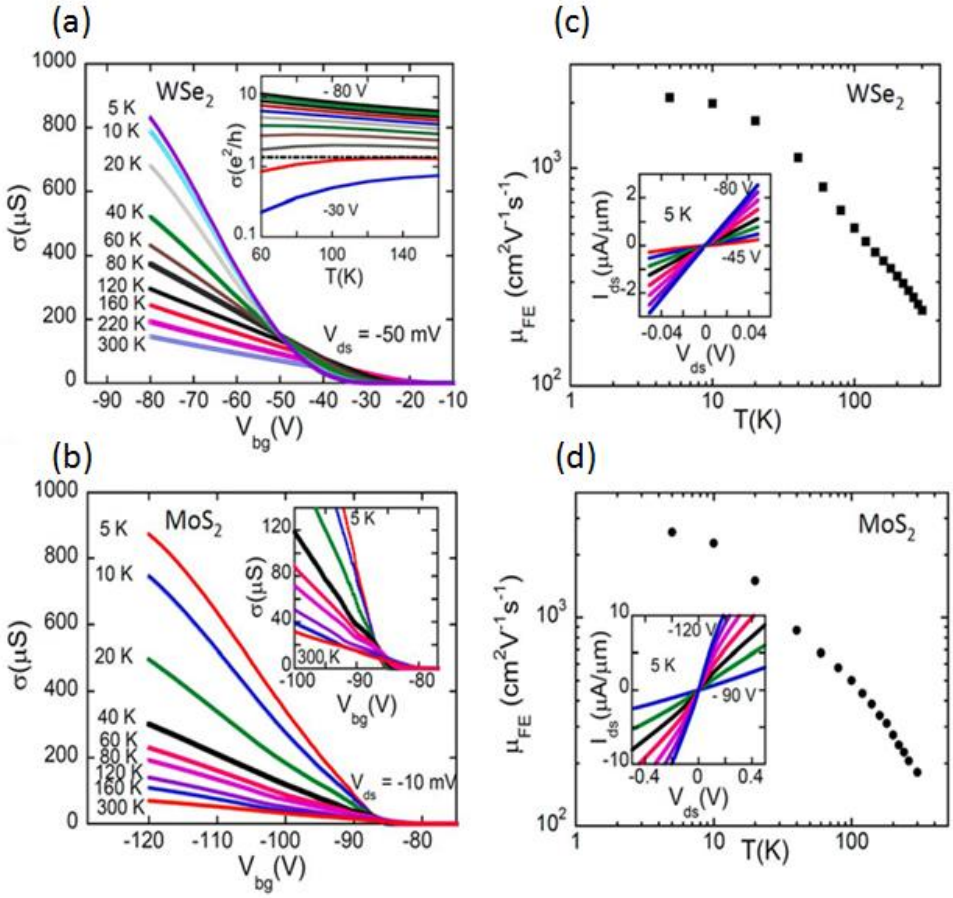


Figure 4.2 Intrinsic channel properties observed in WSe_2 (a,) (c) and MoS_2 (b,) (d) devices with 2D/2D contacts. (a) Temperature-dependent two-probe conductivity vs. V_{bg} at V_{ds} = -50 mV. Inset: the temperature dependence of conductivity at gate voltages in the range of -30 V to -80 V in steps of –5 V. MIT is also observed at ~e^2/h as indicated by the dashed line. (b) Temperature-dependent two-terminal conductivity of MoS_2 as a function of V_{bg} at V_{ds}= -10 mV. Inset: conductivity within the MIT region on an expanded scale. (c,) (d) Temperature-dependence two-terminal field-effect hole mobility μ_{FE} in WSe_2 (c) and MoS_2 (d). The highest two probe field effect mobility is observed in two-terminal measurements where $\mu_{FE} \approx 2.0\times10^3$ $cm^2V^{-1}s^{-1}$ in WSe_2 and $\mu_{FE} \approx 2.8\times10^3$ $cm^2V^{-1}s^{-1}$ in MoS_2 at 5K. The linearity of the output characteristics of WSe_2 and MoS_2 devices, shown in the insets of (c,) and (d,) the highly ohmic out-put characteristic indicates the absence of Schottky barriers in the contact region.

As the temperature decreases from 300K to 5 K, the hole mobility of the WSe_2 device increases from ~2.2×10^2 $cm^2V^{-1}s^{-1}$ to about 2.1×10^3 $cm^2V^{-1}s^{-1}$. This mobility increase with decreasing temperature, along with the large mobility values, strongly suggests intrinsic phonon limit channel properties.

4.3.3 Device Performance of p-MoS_2

The major challenge to fabricate high-quality p-type MoS_2 devices[139-141] is caused by the hole injection at the metal/MoS_2 interface region obstructed by a large Schottky barrier, which forms during the common alignment of the metal Fermi level near the conduction band edge of MoS_2.[20] Such high Schottky barriers can be avoided with this new 2D/2D contact strategy, and low-resistance contacts can also be observed from the hole channel of 2D/2D contact MoS_2 FET devices. Figure 4.2(b) shows the two-terminal conductivity as a function of back gate voltage for MoS_2 FET device which consists 6.8 nm thick MoS_2 as a channel, and degenerately p-doped MoS_2 ($Nb_{0.005}Mo_{0.995}S_2$) as drain and source electrodes. In contrast to MoS_2 devices with conventional metal contacts, which display n-type behavior, the above MoS_2 device exhibits p-type behavior. The MIT is also observed in the temperature-dependent conductivity of the p-type MoS_2 device, as seen in the inset of Fig. 4.2(b.) We observe the on-state conductivity increase nearly ~13 fold as the temperature decreases from 300 K to 5 K, and in the inset of Fig.4.2(d) a

linear output characteristics also been revealed down to 5 K also indicates a barrier-free contact with a low contact resistance. As seen in Fig. 4.2(d), the two terminal field-effect hole mobility of the MoS_2 device increases from ~1.8×10^2 $cm^2V^{-1}s^{-1}$ to about 2.8×10^3 $cm^2V^{-1}s^{-1}$ as the temperature decreases from 300K to 5 K. This low-temperature mobility values achieved in our p-type WSe_2 and MoS_2 devices represent record high two-terminal hole mobility values in few-layer TMDs.[116,117,142] We found both hBN channel passivation and low-resistance 2D/2D ohmic contacts are essential to improve to such high two-terminal extrinsic mobility values. With the promising results presented above, we further quantify the contact resistances of the 2D/2D contacts using the transfer length method (TLM). The following section shows the characterization of electrical contacts between metal/p-doped WSe_2, metal / p-doped WSe_2 /undoped Wse_2, follow with the short channel performance further indicate the superior property of the device enabled by the 2D/2D contact strategy.

4.3.4 Characterization of electrical contacts between metal (Ti/Au) and degenerately p-doped WSe_2

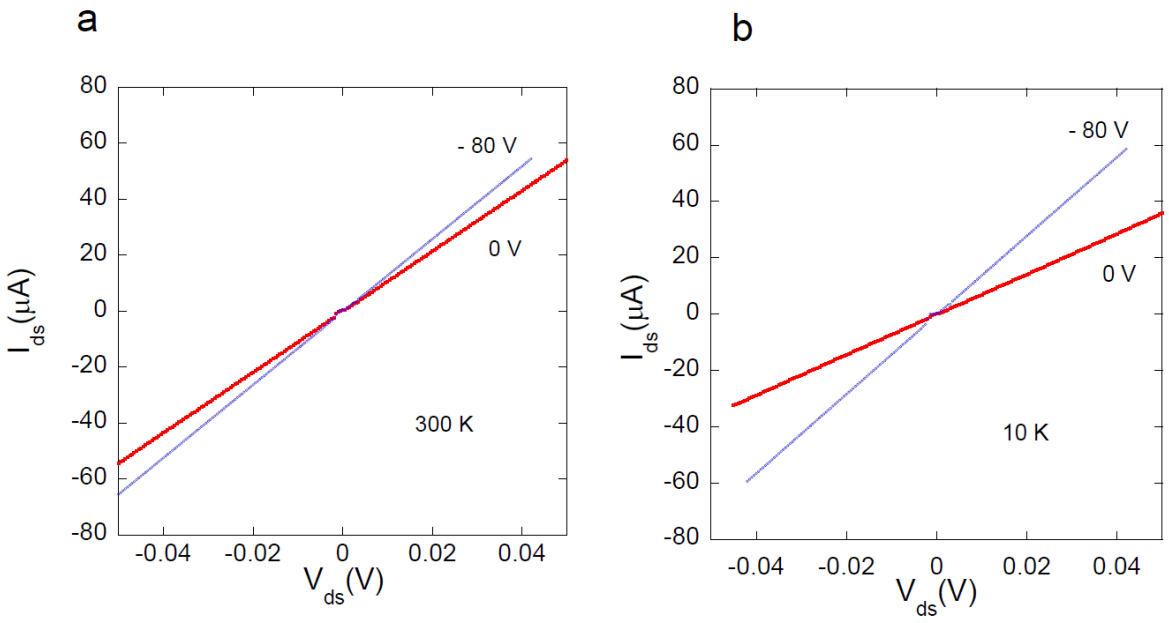


Figure 4.3 I-V Output characteristics of a 12nm thick Nb-doped WSe_2 with Ti/Au contacts measured at (a) 300 K and (b) 10 K. The highly linear I_{ds}-V_{ds} behavior from room temperature

down to cryogenic temperatures indicate barrier-free ohmic behavior. Also the weak gate voltage dependence and weak temperature dependence of the drain-source current are consistent with degenerate p-doping.

The Fig. 4.3 is shown the highly ohmic I-V output characteristics of degenerate p-doping WSe_2 device which is ascribed to the very thin and highly transparent depletion layer at the interface between heavily doped semiconductor, Nb-WSe_2 and Ti/Au metal electrode. The I_{ds} displays slightly increases as the gate voltage increases from 0 V to -80 V, indicating strong p-doping. From the result of Fig. 4.3 which I_{ds}-V_{ds} characteristics show weak temperature dependence also suggest the absence of carrier freeze-out consistent of degenerate doping.

4.3.5 Contact Resistance and short channel performance

In order to further quantify the contact resistance **(**R_C**)**, we here present the transfer line method (TLM) measurements showing in the Figures 4.4(a,)(b,) the schematic diagram and an optical micrograph of a WSe_2 test structure for TLM measurements, it consists an ~7 nm thick undoped WSe_2 channel, outlined by the white dashed line, connected to ~21 nm thick p-doped WSe_2 ($Nb_{0.005}W_{0.995}Se_2$) drain and source contacts with varying gap separation, outlined by the yellow dotted lines. In the result of I-V out-put measurement (Fig 4.4 (c)), the y intercept of the linear fit to the total resistance as a function of the channel length, we extract a R_C of ~ 0.23 - 0.34 kΩ μm, which varies slightly on the gate voltage. The result of low R_C enabled by the 2D/2D contact strategy is significantly lower than our previous result in chapter 3 where device with graphene/WSe_2 contacts (R_C ~2 kΩ μm).[2] And compares favorably with the best results achieved on TMD devices (~ 0.2 - 0.7 kΩ μm).[119,121] Moreover, when decreasing temperature to 150 K, the R_C increases slightly only to ~0.6 kΩ μm, with further decreasing temperature R_C remains nearly constant, as shown in the inset of Fig. 4.4(c,) suggest that highly transparent 2D/2D contacts and that current is injected with the absence of thermionic emission of charge

carriers. Since the R_C is significant reduced, it is expected resulting in substantially improvement of the device performance.

In Figure 4.4(d,) it shows the out-put characteristics of a short-channel WSe_2 device where the L ≈ 0.27 μm, W ≈ 0.50 μm, which is part of the test structure for TLM measurements (Fig. 4.4(a).) The device exhibits with the comparable large drive currents exceeding 320 μA $μm^{-1}$ to the highest drive currents achieved in few-layer TMD devices.[6]

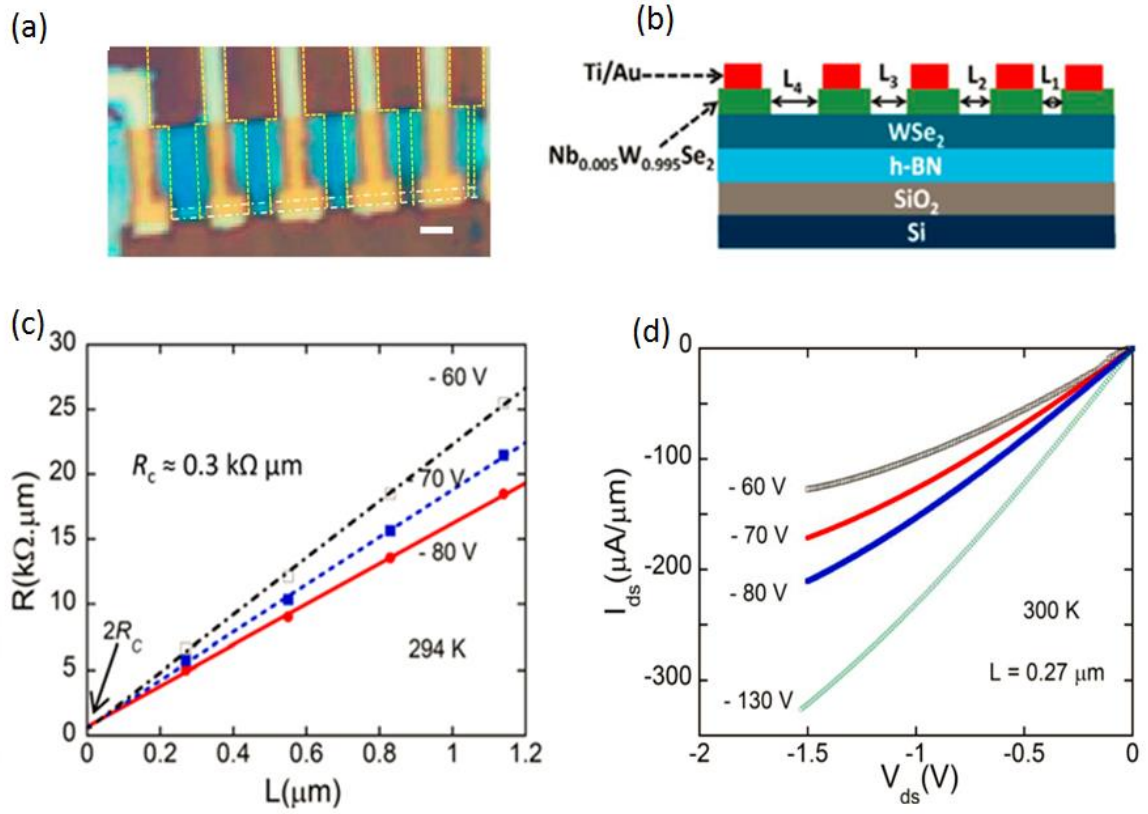


Figure 4.4 Performance of a few layer WSe_2 FET with highly p-doped WSe_2 ($Nb_{0.005}W_{0.995}Se_2$) 2D/2D contacts for TLM. (a) Optical image of the WSe_2 TLM structure. (b) Schematic side view of a test structure for TLM measurements. The contours of the WSe_2 channel are marked by the white dashed lines, and those of the $Nb_{0.005}W_{0.995}Se_2$ contacts by yellow dash-dotted lines. The metal electrodes (Ti/Au) for electrical connections are deposited on top of the $Nb_{0.005}W_{0.995}Se_2$ contacts. The thickness of the device channel is ~ 7.0 nm. White scale bar represent 1 μm in (a). (c) shows total resistance R which multiplied by the channel width as a function of channel length L. The intercept of the linear fit on the vertical axis represents the contact resistance $2R_C$. (d) Output characteristics of the shortest channel (L ≈ 0.27 μm). The maximum drive current reaches around 320 μA/μm at V_{ds} = - 1.5 V and V_{bg} = -130 V.

It is worth to indicate that at the large values V_{bg} = -130 V and V_{ds} = -1.5 V, the drive current I_{ds} (Fig. 4.4(d)) has not yet reached saturation, which indicates that even higher drive currents can be further achieved.

Since the measured effective contact resistance R_C in Fig. 4.4(c) is the series resistance of, the layer resistance of the channel material underneath the drain/source contacts (RCh-layer), the 2D/2D junction contact resistance (RC-2D/2D), the layer resistance of the TMD drain/source (RC-layer), and the metal contact resistance (RMC).

In order to optimize the 2D/2D contacts, it is important to separately determine these constituent resistances. Particularly, it is critical to determine RMC, the contact resistance between the Ti/Au electrodes and degenerately p-doped WSe_2. Fig. 4.5(a) shows optical image of a device structure used to extract the RMC, where the channel length is defined as the separation space between adjacent metal electrodes.

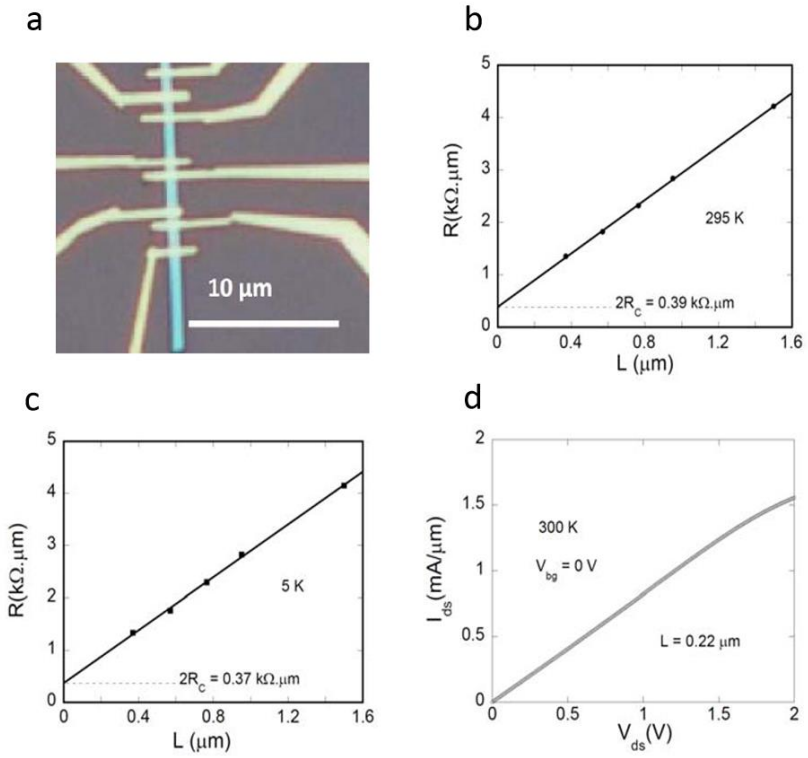


Figure 4.5 (a) Optical image of a device of TLM measurement with a ~18 nm thick degenerately p-doped WSe_2 ($Nb_{0.005}W_{0.995}Se_2$) with Ti/Au metal contacts. Normalized total resistance as a function channel length measured at 295K (b), and 5 K (c). (d) I-V output characteristic at 0 V back gate voltage.

The sum of contact resistance RMC and channel resistance is measured between any adjacent pair of electrodes. By plotting the total resistance as a function of channel length, both contact and channel resistance can be respectively determined for a uniform channel with consistent contacts. Fig. 4.5 (b,) (c) show the normalized total resistance as a function of channel length for the device measured 300K and 5 K. From the intercept of the linear fit, we extract the contact resistance RMC ~ 0.20 kΩ μm and 0.19 kΩ μm for 300K and 5 K, respectively. All RMC (0.18 - 0.20 kΩ μm) is observed for the entire temperature range between 300 K and 5 K, which strongly indicates that the contacts between the highly p-doped WSe_2 and Ti/Au are ohmic, and low resistance contact. The low RMC also result to high drive current. Fig. 4.5(d) shows the I-V output characteristic for a short channel of p-doped WSe_2 with a channel length of ~ 0.22 μm. As a result, a high drain current of > 1.5 mA/μm at V_{ds} = 2 V and Vbg = 0 V is revealed.

Due to the effective contact resistance RC (~ 0.3 kΩ μm) in Fig. 4.4 which also includes a metal/p-doped-WSe_2 contact resistance of ~ 0.2 kΩ μm, the actual 2D/2D contact resistance in between highly p-doped WSe_2 and undoped WSe_2 channel is expected to be ~ 0.1 kΩ μm or less, and similar RC is also achieved in another WSe_2 device with 2D/2D homo-contact with a 9.2 nm thick channel. Fig. 4.6(a,) (b) shows the optical image of a 9.2 nm thick WSe_2 channel with highly p-doped WSe_2 contacts and different channel length between adjacent pairs of p-doped WSe_2 contacts. Fig. 4.6(c) shows the y intercept of the linear fit to total resistance which the contact resistance of ~ 0.3 kΩ μm we extract are in excellent agreement with the result in Fig. 4.4, the gate field tuning of the channel Fermi level becomes less effective as the thickness of the channel increases, mainly because of the increased screening of the gate field by the carriers in

the channel.[131] As a result, in thicker samples, the barrier at the 2D/2D interface between the degenerately doped drain/source and the channel cannot be completely eliminated, which will lead to a increase of the 2D/2D interface resistance RC-2D/2D.

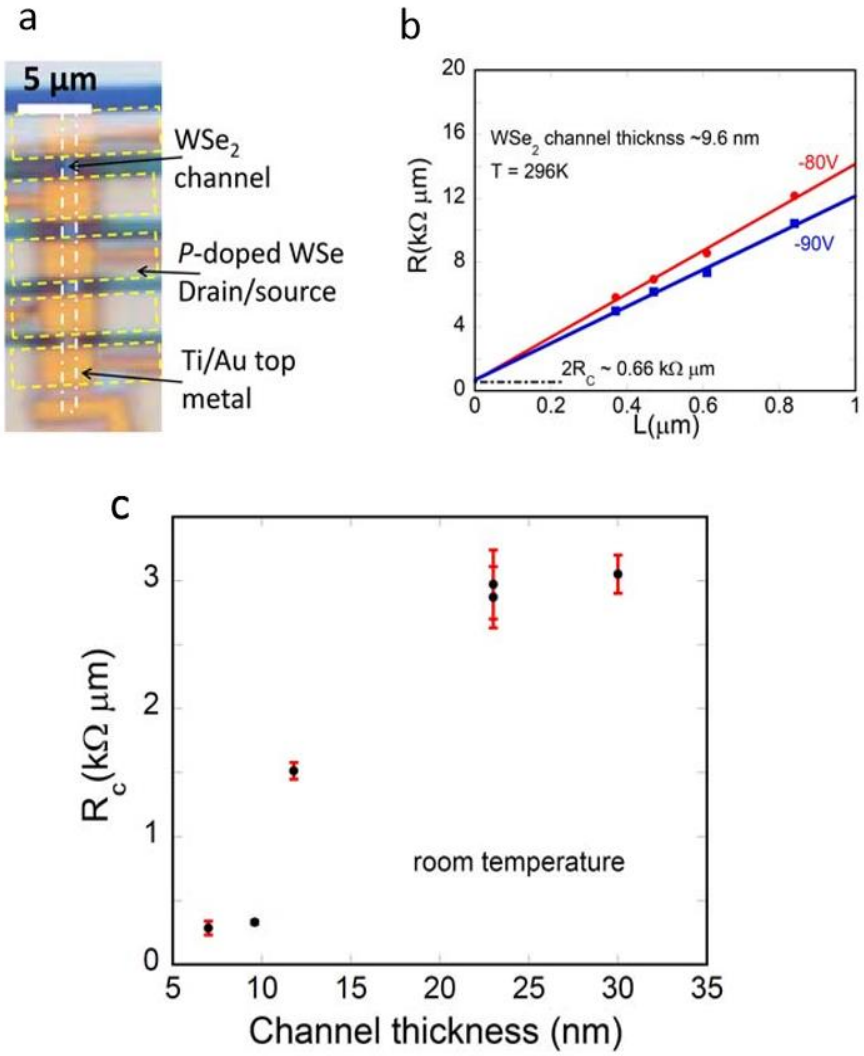


Figure 4.6 (a) Optical micrograph of WSe_2 (9.2 nm thickness) with 2D/2D homo-contacts for TLM measurement, (b) total resistance R versus channel length L. The intercept of the linear fit on the total resistance indicates the contact resistance 2RC. (c) Contact resistance as a function of the channel WSe_2 thickness.

Moreover, we observed the layer resistance of the channel material underneath the drain/source contacts RCh-layer increased as the channel thickness increases. Fig. 4.6(c) shows

the RC as a function of the channel WSe_2 thickness. When the channel thickness is below 10 nm, the effective contact resistance RC is ~ 0.3 kΩ μm, and as the channel thickness increases beyond 10 nm, the effective contact resistance increases rapidly with the channel thickness. The contact resistance of the 30 nm thickness devices reaches ~ 3 kΩ μm at a channel due to the increased charge carrier screening and RCh-layer. Therefore, in order to obtain low 2D/2D contact resistance, thin channel less than 10 nm is needed.

However, as the thickness of the TMD channel thickness reduces to a monolayer, the valley degeneracy tends to decrease by a factor of 3, resulting in corresponding decrease of the density of states (DOS).[144] The reduced availability of states for charge injection in a monolayer TMD channel may result in higher 2D/2D junction resistance and significantly reduce the drive current compared to multilayer channels.[145] As a result, we focus on few-layer TMD channels in our study

4.3.6. Transfer and output characteristics of a top-gated WSe_2 device with vertical 2D/2D contacts

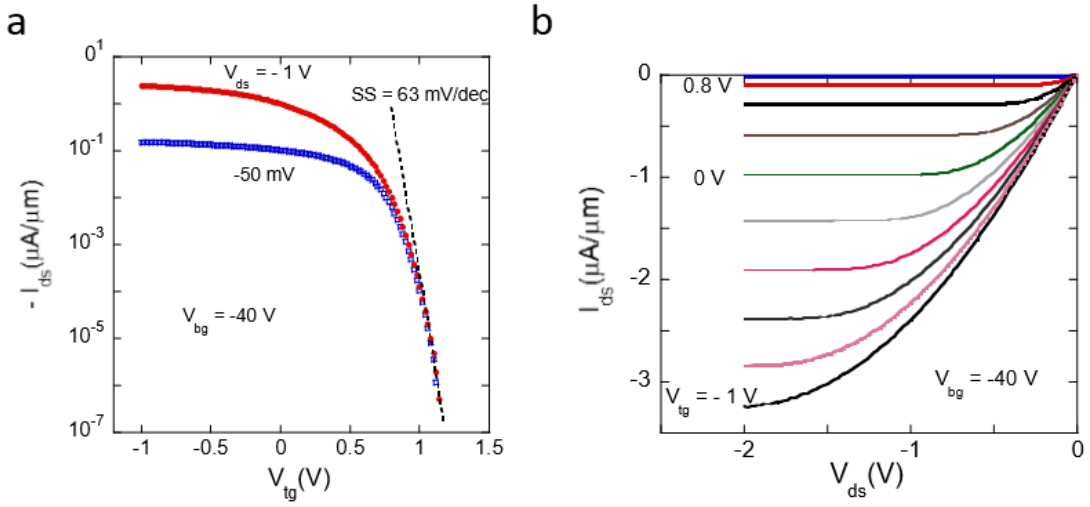


Figure 4.7 Room temperature transfer (a) and output (b) characteristics of a 3.5 nm thick WSe_2 FET device with degenerately p-doped WSe_2 as drain and source contacts along with the hBN as a top gate electrode. With back gate of - 40 V was applied to achieve ohmic drain/source contacts and turn on the underlap of the top-gate and channel region and drain/source contacts.

Figure 4.7 shows the transfer and output characteristics of a top-gated WSe_2 device with highly p-doped WSe_2 as contacts, where a 10 nm thick h-BN crystal is used as top-gate dielectric and Ti/Au is used as the top-gate electrode. A constant back-gate voltage is applied here to electrostatically dope and turn on the under-lapped regions of the top-gate and drain/source contacts. As shown in Fig. 4.7(a,) the transfer characterizes at room temperature shows a nearly ideal subthreshold swing (SS), approaching the theoretical limit of ~ 60 mV/dec for a MOSFET, and in Fig. 4.7(b,) the device displays clear current saturation at high drain/source voltages due to channel pinch-off. At relatively low bias voltages, the linear behavior indicates ohmic contacts.

4.3.7 Hysteresis-free transfer curves of a p-type WSe_2 with vertical 2D/2D drain/source contacts.

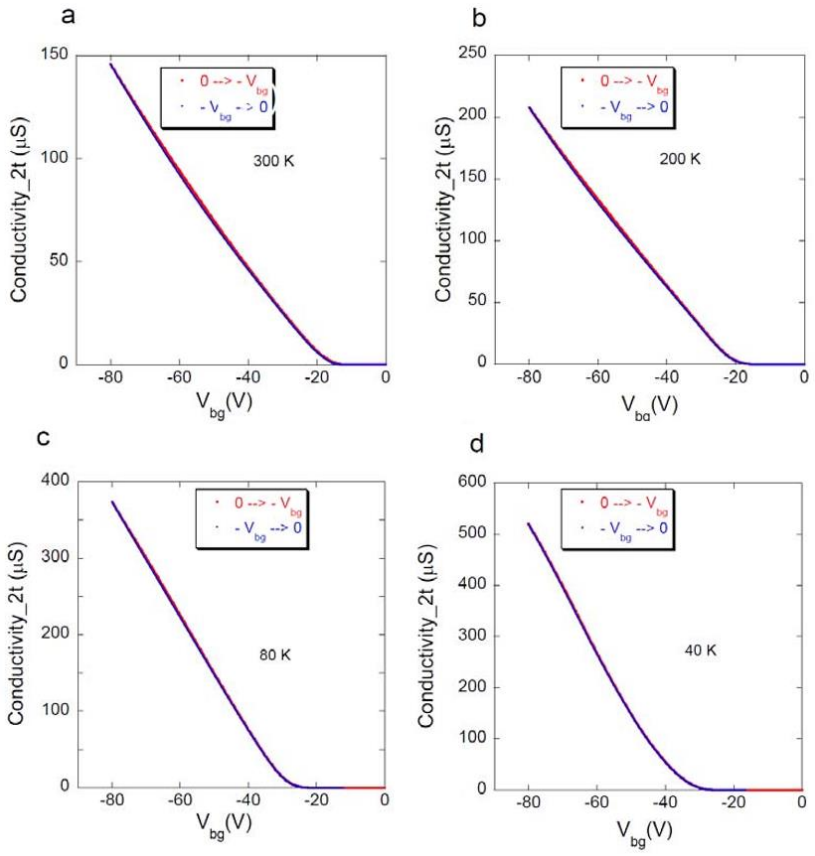


Figure 4.8 Transfer curves of the WSe_2 device (same device in Fig. 4.2) with dual sweep measured at 300 K (a), 200 K (b), 80K (c), and 40 K (d).

Figure 4.8 shows the two-terminal conductivity as function of gate voltage of the device in Fig. 4.2 with the gate voltage swept along opposite directions (dual sweeping mode). The hysteresis is negligibly small at 300 K, which decreases with temperature and essentially disappears below 80K.

4.3.8 Comparison of geometric back gate capacitance with the back gate capacitance determined by Hall effect measurement

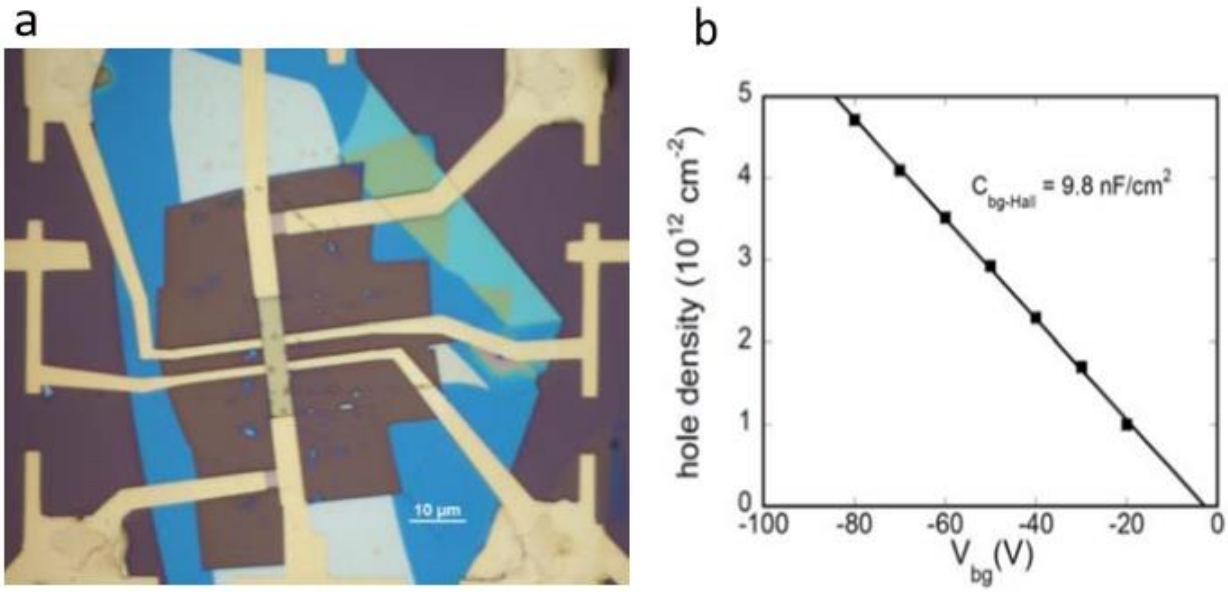


Figure 4.9 (a) Optical image of WSe_2 Hall bar device with h-BN encapsulated and highly p-doped WSe_2 as contacts. (b) The back gate capacitance was extracted from hole density as a function of back gate voltage at 300 K to determine, where hole density was extracted from Hall effect measurement.

Fig. 4.9(a) shows hBN as an encapsulation material from top and bottom a Hall device with a WSe_2 as channel and p-doped WSe_2 as contacts, the Si substrate with 285 nm of thermal oxide. The Hall bar structure was constructed by placing degenerately p-doped WSe_2 thin flakes around the edge of an undoped WSe_2 flake (formed 2D/2D contacts) sandwiched in between a bottom h-BN substrate and a top encapsulation h-BN flake which covers the center part of the TMD flake to preserve the channel property,[136] follow with the metal deposition on top of the p-doped TMD contacts, and the stack was shaped into a Hall bar geometry by using SF6 etching

with EBL patterned mask. The thickness of WSe_2 channel, and the top and bottom h-BN passivation layer is 22 nm thick, 20 nm and 30 nm, respectively. The geometric back-gate capacitance of hall bar device is determined to be ~10.8 nF/cm^2 from the parallel plate capacitor model by using dielectric constant of 3.5 for h-BN.[125,138] We then performed Hall-effect measurement to calculate the charge density as a function of back-gate voltage in order to extract the back gate capacitance. The slope of Fig. 4.9(b) shows the hole density as a function of back-gate voltage at 300 K by Hall measurement, the gate dependence of hole density yields a back gate capacitance $C_{bg\text{-}Hall}$ = 9.8 nF/cm^2, which is in excellent agreement with the geometric capacitance.

We not only present results on p-type TMD transistors in this work, but we have also achieved n-type behavior using heavily n-doped TMDs as drain and source contacts. This is an important advantage of the proposed 2D/2D contact strategy, because availability of both p-type and n-type 2D transistors with low-resistance ohmic contacts is crucial for practical applications.

4.3.9 Electrical characteristics of an n-type WSe_2 device with Re-doped WSe_2 as drain/source contacts

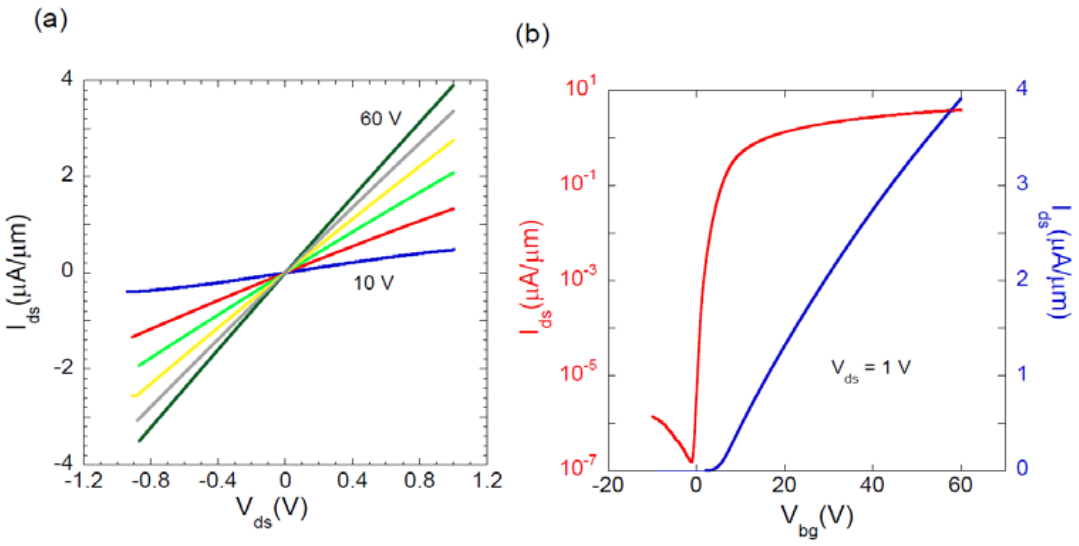


Figure 4.10 The output (a) and transfer (b) characteristics of a 8.5 nm thick n-type WSe_2 FET device with highly n-doped WSe_2 as drain/source contacts under room temperature. Both linear (blue curve) and log (red curve) plots are shown in (b)

The device shows clear n-type of behavior as shown in Fig. 4.10 at room temperature, the linearity of output characteristic at all back gate voltages indicates ohmic contacts as well as the transfer curve shows an high on-off ratio over 10^7 for electrons (Fig. 4.10). The much smaller threshold voltage of the electron side than the hole side for WSe_2 suggests slightly n-doping in our WSe_2 crystals.

4.3.10 Device Stability

Device Stability is show in Figure 4.11, where two-terminal conductivity as a function of gate voltage of an hBN encapsulated WSe_2 device with highly p-doped WSe_2 contacts measured at 300 K in the PPMS. No significant difference is observed between the original measurement (red curve) and a measurement following three weeks of air exposure (blue curve), indicating excellent air stability of the device.

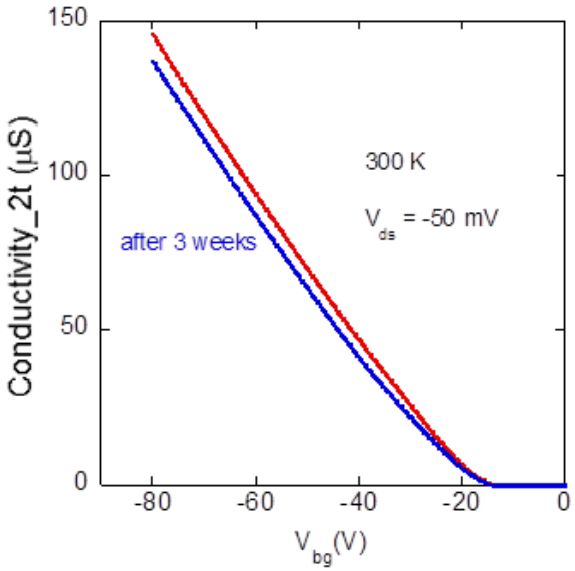


Figure 4.11 The comparison of the transfer curves (red and blue) shows the WSe_2 devices with Nb-WSe_2 drain/source contact demonstrates the device stability following three week apart.

4.3.11 Device Performance improvement

Since we have successfully achieved low resistance contact device with the 2D/2D contact method, we conclude the contact is no longer a dominated factor, therefore, we further testified and found that with improvement of the TMDs single crystal quality, and it leads to the improvement of device performance and channel mobility. It further conforms the channel mobility is limited by the channel impurity not by the contact, showing in Fig. 4.12**.**

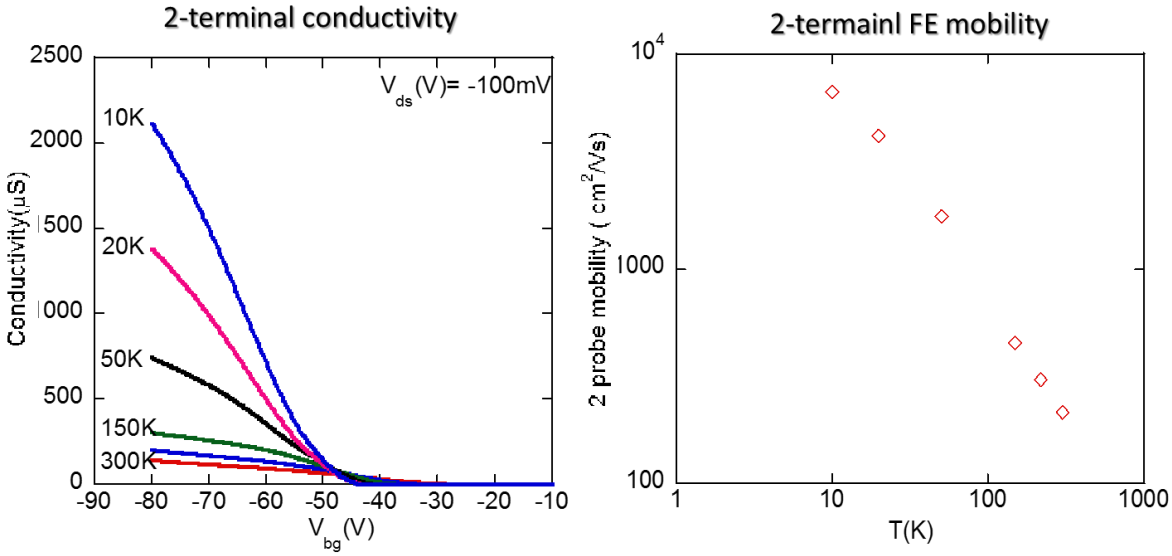


Figure 4.12 the transfer characteristic (left), and two terminal FE mobility as a function of temperature (right) shows the evidence that device performance is limited by channel not contact, as well as the performance is significant improved when improving quality the TMDs (channel).

From the measurement of two terminal conductivity as a function of back-gate voltage with temperature from room temperature down to the 10K shows clearly the phono limit intrinsic channel property, as well as the 2 probe mobility reach as high as 6600cm $^{2}V^{-1}$ S^{-1} at 10K. Note, we have also fabricated several WSe_2 FETs device with the same thickness range of 7nm with the better quality of TMDs single crystals, as a result the range is in between 3000 to 6600cm $^{2}V^{-1}$ S^{1} down to cryogenic temperature.

To sum up, we have developed a novel strategy for 2D/2D contact to achieve high-quality ohmic contacts for MoS_2, $MoSe_2$ and WSe_2 FETs. The low-resistance ohmic contacts drastically improved devices performance which include the following, on/off ratios up to $>10^9$, drive currents >320 μA μm^{-1}, and two-terminal extrinsic field-effect mobility up to 2.8×10^3 $cm^2V^{-1}s^{-1}$ at cryogenic temperatures. This newly developed contact engineering approach can be applied to a wide range of 2D materials for both p-type and n-type transistors and are also compatible to conventional semiconductor processes, and may be implemented in roll-by-roll production of flexible electronics.

4.3.12 Summary of electrical characteristics of additional WSe_2 and MoS_2 device with homojunction vertical 2D/2D contacts

Device label	Channel/Contacts	Channel thickness (nm)	Length/ Width (μm)	$\mu_{FE}(cm^2/Vs)$ at RT and 80K	On/off ratio at RT V_{ds} = -1V
[2-15-5]_No3 04_12	WSe_2/p-WSe_2	4.0	5.3/8.4	170 (RT) 380(80 K)	10^7
[2-15-15]_No3 _5-3_12	WSe_2/p-WSe_2	3.0	3.2/6.2	150 (RT) 490(80 K)	10^8
[3-23-15]_No1 _2-5_12	WSe_2/p-WSe_2	10	20/1.8	200 (RT) 580(80 K)	10^6
[3-23-15]_No2 _-2-5_12	WSe_2/p-WSe_2	10	37.4/5	240 (RT) 630(80K)	10^7
[4-4-15]_No3 -25_12	WSe_2/p-WSe_2	3.5	14.8/4.7	250 (RT) 620(80K)	10^9
[4-4-15]_No3 55_12	WSe_2/p-WSe_2	3.5	10.8/3.0	200 (RT) 540 (80K)	10^9
[5-29-15]_No.1 46_12	WSe_2/p-WSe_2	6.4	14.5/3.3	230(RT) 700(80K)	10^6

[7-12-15]_No.1 -60_12	MoS_2/p- MoS_2	6.8	13/2.7	180(RT) 550(80K)	10^7
[3-18-15]_No.3	MoS_2/p- MoS_2	18	10.5/4.4	120(RT)	10^6
[07-09-15]_No.1 -33_22	MoS_2/p- MoS_2	6.0	12.5/7.4	200(RT) 700(80K)	10^6

Table 1 It shows all 2 terminal 2D/2D homojunction device with the list of the device channel dimensions, 2 terminal field effect mobility from room temperature to 80K, and on/off ratio of the device.

CHAPTER 5 CONCLUSION AND FUTURE WORK

5.1 Conclusion

We have developed novel contact methods to form low resistance contacts to TMDs.

1) We have used graphene as a work function tunable electrodes and tuned the electrical contacts with an ionic liquid gate[1]. As a result, we have fabricated WSe2 FETs with an ON/OFF ratio of $>10^7$ at 170 K, large electron mobility of ~330 $cm^2V^{-1}s^{-1}$ and hole mobility of ~270 $cm^2V^{-1}s^{-1}$ at 77 K, and resistance contact of ~ 2kΩ μm.

2) To further improve the contacts and thus device performance, we have used degenerately doped WSe_2 and MoS_2 as contact materials for undoped WSe_2 and MoS_2 as channel materials through vdW assembly. WSe_2 FET devices with degenerately doped WSe_2 contacts exhibit low contact resistances of ~0.3 kΩ μm, on/off ratios up to > 10^9 as well as two-terminal field-effect hole mobility $\mu_{FE} \approx 2\times10^2$ $cm^2\,V^{-1}\,s^{-1}$ at 300K, which increases to > 6×10^3 $cm^2\,V^{-1}\,s^{-1}$ down to 10K. The 2D/2D low-resistance ohmic contacts presented here represent a new device paradigm that overcomes a significant bottleneck in the performance of TMDs and other 2D materials as the channel materials in post-silicon electronic. To the best of our knowledge, the low-temperature mobility values observed here represent record high two-terminal hole mobility in few-layer TMDs.[49, 50, 77]

5.2 Future work

The low-resistance ohmic contacts achieved using the novel 2D/2D contact strategy place us in a unique position to i) study the intrinsic transport properties and scattering mechanisms in TMD channels, and ii) to explore the rich quantum physics in TMD 2DEGs and 2DHGs.

The hall bar structures of few-layer and monolayer TMDs with 2D/2D contacts by placing degenerately doped TMD thin flakes around the perimeter of an undoped TMD flake sandwiched

between a bottom h-BN substrate and a top h-BN that covers the center part of TMD flake will be one of the main focus in the next step. 2D/2D contacts are then formed between the doped TMD flakes and the exposed edge areas of the undoped TMD flake.[136] Subsequently, metal electrodes will be fabricated on top of the doped TMD contacts, and the stack will be shaped into a Hall bar geometry such that the h-BN encapsulated TMD will form the channel. Four-terminal conductivity and Hall mobility will be measured as a function of gate voltage (carrier density) for a wide temperature range down to 2K in a Physical Property Measurement System (PPMS) to understand the scattering mechanisms and the performance limit of TMDs as channel materials. The temperature and carrier-density dependence of the Hall mobility will be compared with theoretical modeling to evaluate the relative contributions of the electron-phonon scattering and other extrinsic scattering mechanisms such as the charged impurity scattering. The ultimate performance limit of h-BN encapsulated TMD channels is expected to be influenced by the defect density and/or the purity of the starting TMD crystals. We will also study the temperature and magnetic field dependence of Shubnikov-de Haas oscillations in h-BN encapsulated TMDs with 2D/2D contacts to extract important information about the electronic structure of these systems, such as cyclotron mass, quantum scattering time, and level degeneracy. Other emerging quantum phenomena such as quantum Hall effects will also be explored.

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ABSTRACT

TWO-DIMENSIONAL LOW-RESISTANCE CONTACTS FOR HIGH PERFORMANCE WSe_2 and MoS_2, TRANSISTORS

by

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Two-dimensional layered materials beyond graphene such as transition metal dichalcogenides (TMDs) have attracted a lot of interests due to their superior property in many aspects. In this work, I am focusing on two TMD materials: WSe_2 and MoS_2. The main objective this work is to develop novel approaches to fabricating low-resistance ohmic contacts to TMDs for low power, high performance electronic applications. First, we used graphene as electrical contacts for WSe_2 field-effect transistor with superior performance, including a high ON/OFF ratio of $>10^7$ at 170 K, large electron mobility of ~330 $cm^2V^{-1}s^{-1}$ and he hole mobility of ~270 $cm^2V^{-1}s^{-1}$ at 77 K, and low contact resistance of ~ 2kΩ μm. Second, we developed a novel 2D to 2D contacts strategy[2] for a variety of TMDs by van der Waals assembly of substitutionally doped TMDs as drain/source contacts and TMDs with no intentional doping as channel materials. The high intrinsic behavior of the device is revealed, where it exhibits low contact resistances of ~0.3 kΩ μm, on/off ratios up to > 10^9 as well as two-terminal field-effect hole mobility $\mu_{FE} \approx 2\times10^2$ $cm^2\,V^{-1}\,s^{-1}$ at 300K, which increases to > 6×10^3 $cm^2\,V^{-1}\,s^{-1}$ down to 10K. The 2D/2D low-resistance ohmic contacts presented here represent a new device paradigm that overcomes a

significant bottleneck in the performance of TMDs and other 2D materials as the channel materials in post-silicon electronic.

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